SFP-DD MSA

SFP-DD/SFP-DD112/SFP112 Hardware Specification

for

SFP112 AND SFP DOUBLE DENSITY PLUGGABLE TRANSCEIVER

Revision 5.1

March 11, 2022

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements of the pluggable SFP112 module, Double Density SFP-DD module, and Double Density SFP-DD112 connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Fourte International	MultiLane	ZTE

Change History:

Revision	Date	Changes
1.0	September 14 2017	1st public release.
2.0	September 17, 2018	2nd public release. Added Type 2 module. Changed IntL pin to reserved, Changed TxFault to TxFault/Int Updated drawings to include new key. Added test conditions for insertion removal forces.
3.0	April 10 2019	3rd public release. Added 5 W power class. Added SN, MDC connectors. Deleted requirement that host shall not change the state of LPMode when module is present.
4.0	Withdrawn	
4.1	August 10, 2020	4th public release. Added ResetL, IntL, ePPS, Fault signals. Added timing tables for low speeds signals, soft control and status. Chapter 7-Management Interface is now part of Chapter 4-Electrical Specification. Port mapping, optical connectors, and module color coding moved out of Mechanical and Board Definition Chapter-5 and into a new Chapter-5. Appendix A- Normative Connector Performance Requirements added.
4.2	August 17, 2020	5th public release. Added dual functionality IntL/TXFaultDD signal definition for SFP-DD.
5.0	October 1, 2021	6th public release. Added chapter 5 Electrical Specifications for SFP112, added chapter 8 Mechanical specification of SFP-DD112, added chapter 9 Mechanical Specification of SFP112. Added ePPS/Clock signals definition for SFP-DD/SFP-DD112.
5.1	March 11, 2022	7th public release defined a new improved power supply test method 4.10, squelch level reduced to 50 mV for 112G operation 4.8.2. TWI bus timing removed from chapter 4 as identical timing diagram already included in CMIS.

Foreword

The development work on this specification was done by the SFP-DD MSA, an industry group. The membership of the committee since its formation in May 2017 has included a mix of companies which are leaders across the industry.

The members of the SFP-DD MSA would like to acknowledge the contributions of Edmund Poh. He was an excellent engineer; his technical skills and collaborative attitude will be missed.

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1. Scope

The scope of this specification is the definition of a high density 1-channel and 2-channels modules, cage and connector system. SFP-DD supports up to 100 Gb/s in aggregate over a 2 x 50Gb/s electrical interface. SFP112 supports 100 Gb/s over single electrical lane, and SFP-DD112 supports up to 200 Gb/s in aggregate over a 2 x 100 Gb/s electrical interface. The cage and connector design provides backwards compatibility to SFP+/SFP28 [30], [28] modules which can be inserted into an SFP-DD/SFP-DD112 cage and connector using 1 of the electrical channels. SFP112 cage and connectors are compatible with SFP+/SFP28 modules. Furthermore, SFP112 modules maybe inserted into SFP-DD112 cage and connector using 1 of the electrical lanes.

1.1 Overview of SFP-DD/SFP-DD112/SFP112 Specifications

SFP-DD/SFP-DD112/SFP112 specifications are organized into 10 chapters and one appendix addressing electrical, mechanical, environmental, and management aspects of the module.

- Chapter 1 Scope
- Chapter 2 References and Related Standards and SFF Specifications
- Chapter 3 Introduction
- Chapter 4 Electrical specifications and management interface timing for SFP-DD/SFP-DD112
- Chapter 5 Electrical specifications and management interface timing for SFP112
- Chapter 6 Optical port mapping and optical interfaces
- Chapter 7 SFP-DD Mechanical specifications, printed circuit board recommendations
- Chapter 8 SFP-DD112 Mechanical specifications, printed circuit board recommendations
- Chapter 9 SFP112 Mechanical specifications, printed circuit board recommendations
- Chapter 10 Environmental and thermal considerations
- Appendix A Normative module and connector performance requirements.

2. References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

[1] ANSI FC-PI-6 32GFC (INCITS 533)
[2] ANSI FC-PI-7 64GFC (INCITS 543)
[3] ANSI FC-PI-8 128GFC
[4] ASME Y14.5-2009 Dimensioning and Tolerancing
[5] Common Management Interface Specification (CMIS) 5.1, https://www.oiforum.com/wp-content/uploads/CMIS5p1_Third_Party_Spec.
[6] CS-01242017 CS optical connector and receptacle, see http://www.qsfp-dd.com/optical-connector/
[7] EIA-364-1000 TS-1000B Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Controlled Environment Applications, revision B 2009
[8] EN6100-4-2 (IEC immunity standard on ESD), criterion B test specification
[9] Human Body Model per ANSI/ESDA/JEDEC JS-001
[10] IEC 61754-7-1 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 7-1: Type MPO Connector Family - One Fibre Row)
[11] IEC 61754-20 (Fibre Optic Interconnecting Devices and Passive Components - Fibre Optic Connector Interfaces - Part 20: Type LC Connector Family)
[12] IEEE Std 802.3TM-2018, annex 86A, 83E, and 120E
[13] IEEE Std 802.3cd (50 Gb/s, 100 Gb/s, and 200 Gb/s Ethernet), clause 136 and annex 136A
[14] IEEE Std 802.3ck (100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces)
[15] IEEE Std 1588 Precision Clock Synchronization Protocol PTP, 2019
[16] InfiniBand Architecture Specification Volume 2
[17] JEDEC JESD8C.01 Interface Standard for Nominal 3.0/3.3 V Supply Digital Integrated Circuit (LVCMOS)
[18] NEBS GR-63 Physical Protection Requirements for Network Telecommunications Equipment
[19] NXP UM10204, I2C-bus specification and user manual, Rev 6 – 4 April 2014.
[20] OIF CEI 4.0, CL-13 CEI-28G-VSR, CL-16 CEI-56G-VSR PAM4, and CEI-112G-VSR PAM4 specifications
[21] SFP-DD Management Interface, Rev. 2.0
[22] SN-60092019 SN optical connector and receptacle, see http://www.qsfp-dd.com/optical-connector/
[23] TIA-604-5 (FOCIS 5 Fiber Optic Connector Intermateability Standard- Type MPO)
[24] TIA-604-10 (FOCIS 10 Fiber Optic Connector Intermateability Standard- Type LC)
[25] USC-11383001 MDC optical plug and receptacle, see http://www.qsfp-dd.com/optical-connector/

2.2 SFF Specifications:

[26] INF-8074i SFP (Small Formfactor Pluggable) Transceiver, Rev. 1.0
[27] SFF-8071 SFP+ 1x 0.8 mm Card Edge Connector, Rev 1.1
[28] SFF-8402 SFP+ 1x 28 Gb/s Pluggable Transceiver Solution (SFP28), Rev. 1.1
[29] SFF-8419 SFP+ Power and Low Speed Interface, Rev. 1.3
[30] SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface, Rev. 4.1
[31] SFF-8432 SFP+ Module and Cage, Rev. 5.2a
[32] SFF-8433 SFP+ Ganged Cage Footprints and Bezel Openings, Rev. 0.7
[33] SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers, Rev. 12.4.

2.3 Sources

The SFP-DD MSA SFP-DD Hardware Specification for SFP DOUBLE DENSITY 2X PLUGGABLE TRANSCEIVER can be obtained via the www.SFP-DD.com web site.

3. Introduction

This Specification covers the following items:

- Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.
- Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified.
- Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.
- Thermal requirements
- Management Interface Timing requirements
- Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

- Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.
- Optical signaling specifications are not included in this document but are defined in the applicable industry standards.
- Management Registers.

3.1 Objectives

SFP-DD/SFP-DD112 electrical signals, channel assignments, TWI, timing, and power requirements are defined in Chapter 4. SFP112 electrical signals, TWI, timing, and power requirements are defined in Chapter 5. Optical port mapping and optical interfaces are defined in Chapter 6 to ensure that the pluggable modules and cable assemblies are functionally interchangeable. Implementations compliant to dimensions, mounting and insertion requirements defined in Chapter 7 for SFP-DD bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable. Chapter 8 describes an improved SFP-DD form factor called SFP-DD112 with improved signal integrity for 100 Gb/s per lane operation with an aggregate bandwidth of 200 Gb/s. Chapter 9 describes an improved SFP+ form factor called SFP112 with improved signal integrity for 100 Gb/s per lane operation and with an aggregate bandwidth of 100 Gb/s.

3.2 SFP-DD/SFP-DD112/SFP112 System Overview

The SFP-DD form factor system consisting of a transceiver module, cage and connector provides two channels for high speed signals that can support a two-lane trunked application or two independent single-lane applications. The cage and socket can also accept SFP+/SFP28 and SFP112 modules in which case a single lane channel is supported. To support classic SFP+ modules the electrical connector maintains the twenty contacts row defined for SFP+ modules and adds another twenty contacts row to support a second channel.

In addition to contacts for the high speed data signals, the connector provides contacts for module and channel control and status signals including a pair that form a Two-Wire Interface (TWI) [19] or communication with the module's memory. Contacts for high speed data signals, channel level control and status indicator signals and power supply sources for the SFP module are repeated in the row for the second channel.

Contacts for module level control and status signals in the SFP module remain in place and signals for new module level functions were added to the second row.

New global features and associated signals, Low Power Mode, Reset and Interrupt were added and the memory map for SFP-DD was expanded and reorganized for better alignment with CMIS functionality and structure.

SFP-DD management specifications is based on SFP-DD MIS [21]. SFP-DD112 and SFP112 management specifications are based on CMIS [5].

Within the MIS and CMIS the SFP112 and SFP-DD/SFP-DD112 classic contacts, see Figure 3, are associated as Channel 1 and the SFP-DD/SFP-DD112 additional contacts are associated as Channel 2. Within this document the name, Channel 1, is synonymous with the name SFP “classic” Channel and Channel 2 is synonymous with the name DD “additional” Channel.

Adding a second channel to SFP-DD/SFP-DD112 results in increased module power consumption. Accommodations for the increased consumption include defining additional power classes, defining a Type 2 module and defining an enlarged heat sink seating area with surface flatness and roughness requirements. A low power mode was added to provide the host a means for power management.

Another accommodation for a second channel was the inclusion of addition optical connectors including MPO [10] and [23], duplex LC [11] and [24], see Figure 28.

3.3 Applications

This specification defines a connector, cage and module for single or double lane applications at up to 112 Gb/s (56 GBd) per lane. Intended applications include but are not limited to Ethernet and/or InfiniBand and/or Fibre Channel. The SFP-DD/SFP-DD112/SFP112 interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.

An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the SFP-DD/SFP-DD112/SFP112 modules.

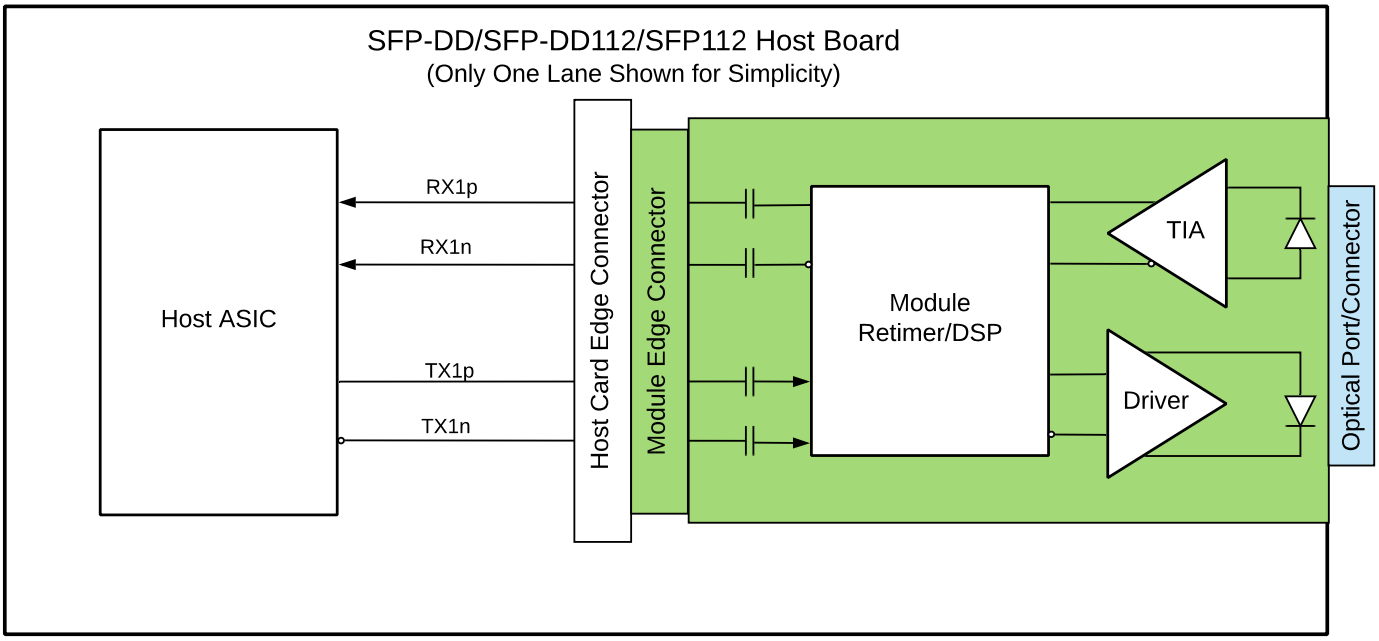


Figure 1: Application Reference Model

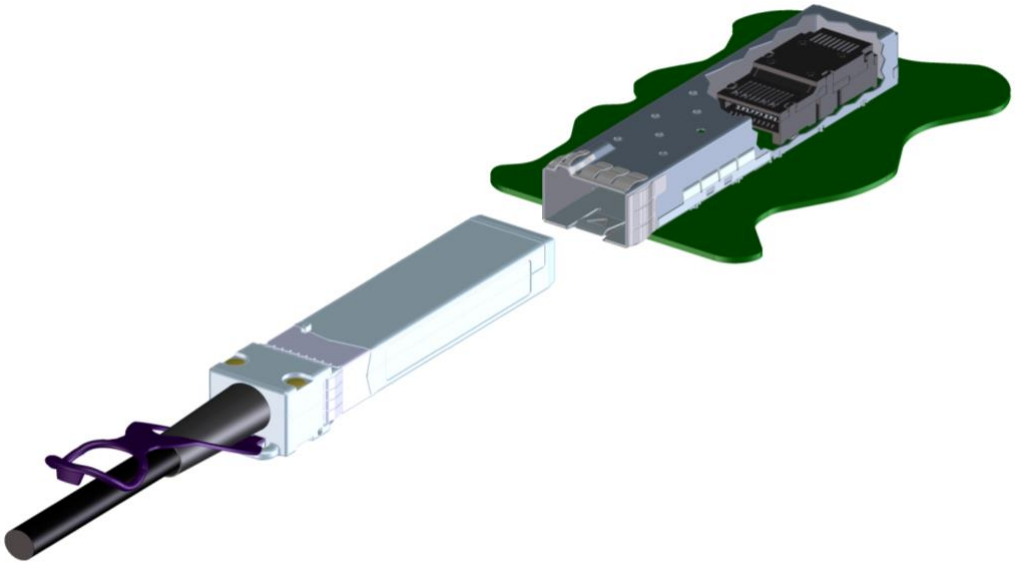


Figure 2: SFP-DD/SFP-DD112/SFP112 Cage, Connector and Module

4. Electrical Specification and Management Interface Timing for SFP-DD/SFP-DD112

This chapter contains signal definitions and requirements that are specific to the SFP-DD/SFP-DD112 modules. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 General Requirements

The SFP-DD/SFP-DD112 modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered.

For EMI protection the signals from the host connector should be shut off when the SFP-DD/SFP-DD112 modules are not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The SFP-DD/SFP-DD112 modules signal ground contacts GND should be isolated from module case. An isolated SFP-DD/SFP-DD112 module case from signal ground provides equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground “GND” of the module.

All electrical specifications shall be met over the entire specified range of power supplies given in section **Error! Reference source not found.**.

4.2 Electrical Connector

The SFP-DD/SFP-DD112 module edge connector consists of a single paddle card with 20 pads on the top and 20 pads on the bottom of the paddle card for a total of 40 pads. The pads positions are defined to allow insertion of either an SFP-DD/SFP-DD112 module or an SFP28 into the SFP-DD/SFP-DD112 receptacle. The classic signal locations are deeper on the paddlecard, so that classic SFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins open circuited in an SFP application.

The pads are designed for a sequenced mating:

- First mate – ground pads
- Second mate – power pads
- Third mate – signal pads.

Because the SFP-DD/SFP-DD112 module has 2 rows of pads, the additional SFP-DD pads will have an intermittent connection with the classic SFP/SFP+ pins in the connector during the module insertion and removal. The 'classic' SFP+/SFP28/SFP112 pads have a “B” label shown in Table 1 to designate them as the first row of module pads to contact the SFP-DD/SFP-DD112 connectors. The additional SFP-DD/SFP-DD112 pads have a “A” label with first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the classic SFP+/SFP28/SFP112 pads and the respective additional SFP-DD/SFP-DD112 pads are simultaneous.

Figure 3 shows the signal symbols and pad numbering for the SFP-DD/SFP-DD112 modules edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 40 pads intended for high speed signals, low speed signals, power and ground connections.

Table 1 provides more information about each of the 40 pads. Figure 40 and Figure 41 show pad dimensions. The surface mount configuration is shown in Figure 46.

For EMI protection the signals from the host connector should be shut off when the SFP-DD/SFP-DD112 module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The chassis ground (case common) of the SFP-DD/SFP-DD112 module should be isolated from the module’s circuit ground, GND, to provide the

equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

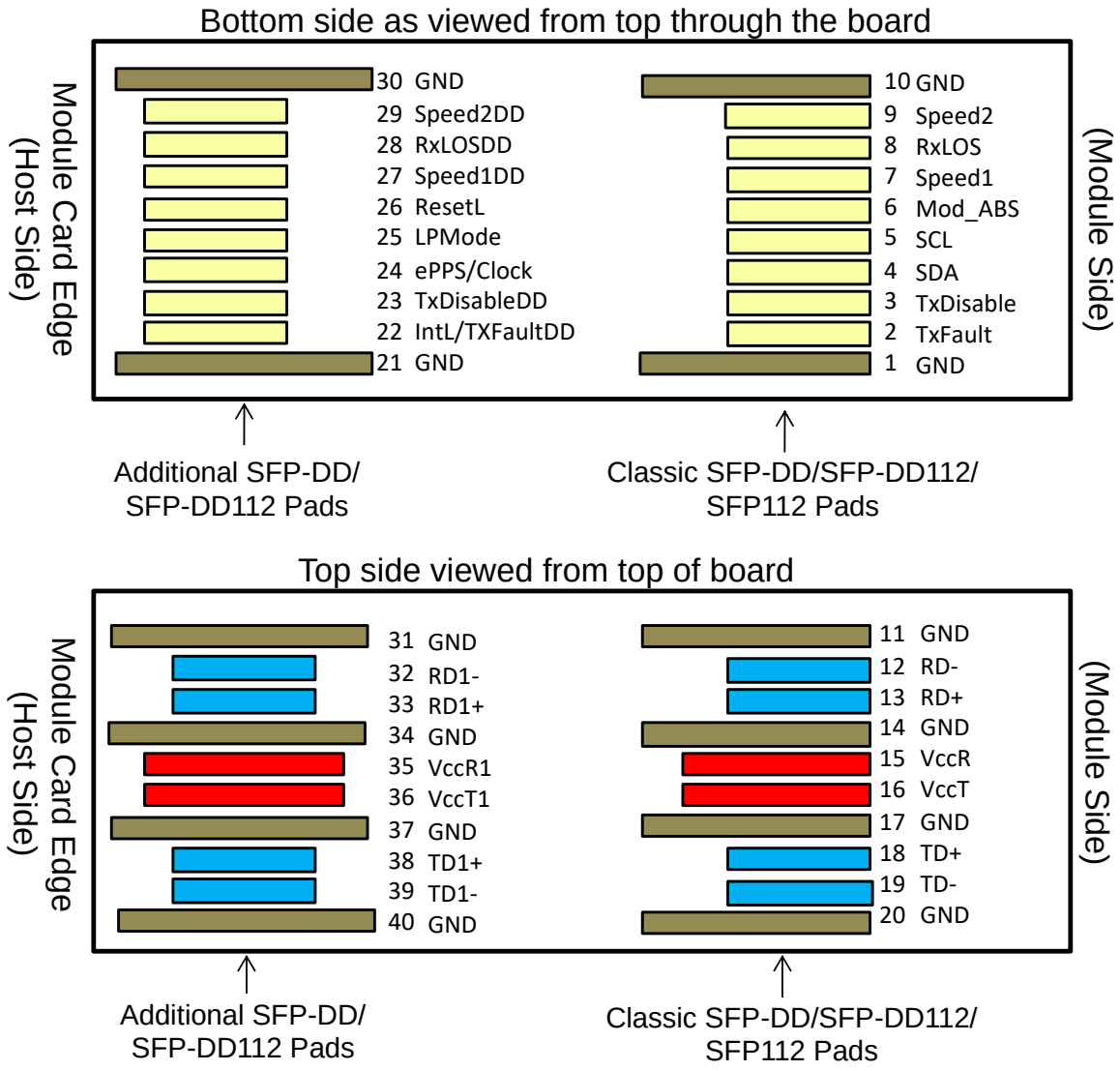


Figure 3: SFP-DD/SFP-DD112 module pad layout

Because the SFP-DD/SFP-DD112 module has 2 rows of pads, the additional SFP-DD/SFP-DD112 pads will have an intermittent connection with the classic SFP pins in the connector during the module insertion and removal. SFP-DD/SFP-DD112 module pads are compatible with SFP+/SFP28 [30], [28] are designated as “classic” pads in Table 1 to designate them as the second row of module pads to contact the SFP-DD/SFP-DD112 connector. The additional module pads are designated as ”DD” pads in Table 1 to designate them as the first row of module pads to contact the SFP-DD/SFP-DD112 connector. The additional SFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the classic SFP pads and the respective additional SFP-DD/SFP-DD112 pads are simultaneous. For a reliable interconnect, a sufficient contact wipe of the connector pins sliding over the module gold pads is required. In the past, long signal pads have been used to provide the mechanical wipe. As operating speeds were relatively slow, the electrical stub was not an issue with signal integrity.

As operating speeds have increased, signal pad lengths have become shorter and shorter to reduce electrical stubs, however this caused insufficient mechanical wipe. A solution is to add a small separation of the signal pad such that there is a passive 'pre-wipe" pad and an active signal pad. In SFP-DD/SFP-DD112, there are also long pre-wipe pads between the additional SFP-DD/SFP-DD112 pads and the classic SFP pads. This provides connector pins a gold platted pad surface over which to slide between rows.

1

Table 1- Pad Function Definition

Pad	Logic	Symbol	Module Pad Descriptions	Plug Sequence[4]	Notes
0		Case	Module case	0	
1		GND	Ground	1B	1
2	LVTTL-O	TxFault	Module Fault Indication: optionally configured as classic SFP Module Fault Indication via TWI as described in the SFP-DD MIS	3B	
3	LVTTL-I	TxDisable	Transmitter Disable for classic SFP channel	3B	
4	LVCMOS-I/O	SDA	Management I/F data line	3B	
5	LVCMOS-I/O	SCL	Management I/F clock	3B	
6	LVTTL-O	Mod_ABS	Module Absent	3B	
7	LVTTL-I	Speed1	Rx Rate Select for classic SFP channel	3B	
8	LVTTL-O	RxLOS	Rx Loss of Signal for classic SFP channel	3B	
9	LVTTL-I	Speed2	Tx Rate Select for classic SFP channel	3B	
10		GND	Ground	1B	1
11		GND	Ground	1B	1
12	CML-O	RD0-	Inverse Received Data Out for classic SFP+ channel	3B	
13	CML-O	RD0+	Received Data Out for classic SFP+ channel	3B	
14		GND	Ground	1B	1
15		VccR	Receiver Power	2B	2
16		VccT	Transmitter Power	2B	2
17		GND	Ground	1B	1
18	CML-I	TD0+	Transmit Data In for classic SFP channel	3B	
19	CML-I	TD0-	Inverse Transmit Data In for classic SFP channel	3B	
20		GND	Ground	1B	1
21		GND	Ground	1A	1
22	LVTTL-O	IntL/ TxFaultDD	Interrupt: optionally configured as TxFaultDD via TWI as described in the SFP-DD MIS	3A	
23	LVTTL-I	TxDisableDD	Transmitter Disable for DD channel	3A	
24	LVTTL-I	ePPS/Clock	Precision Time Protocol (PTP) reference clock input	3A	3
25	LVTTL-I	LPMode	Low Power Mode Control	3A	
26	LVTTL-I	ResetL	Module Reset	3A	
27	LVTTL-I	Speed1DD	Rx Rate Select for DD channel	3A	
28	LVTTL-O	RxLOSDD	Loss of Signal for DD channel	3A	
29	LVTTL-I	Speed2DD	Tx Rate Select for DD channel	3A	
30		GND	Ground	1A	1
31		GND	Ground	1A	1
32	CML-O	RD1-	Inverse Received Data Out for DD channel	3A	
33	CML-O	RD1+	Received Data Out for DD channel	3A	
34		GND	Ground	1A	1
35		VccR1	Receiver Power for DD channel	2A	2
36		VccT1	Transmitter Power for DD channel	2A	2
37		GND	Ground	1A	1
38	CML-I	TD1+	Transmit Data In for DD channel	3A	
39	CML-I	TD1-	Inverse Transmit Data In for DD channel	3A	
40		GND	Ground	1A	1

Notes:

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 12. VccR, VccT, VccR1, VccT1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. The ePPS pins (if not used) may be terminated with 50 Ω to ground on the host.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 0, 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional SFP-DD/SFP-DD112 pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

4.3 Overview of the Low Speed Electrical Hardware Signals

The SFP-DD/SFP-DD112 connector allocates contacts for a set of low speed signals for control, status and management by the host. These include dedicated hardware signals and TWI signals. The dedicated hardware signals are the following:

- TxDisable, TxDisableDD
- RxLOS, RxLOSDD
- Speed1, Speed2, Speed1DD, Speed2DD
- TxFault
- IntL/TXFaultDD
- Mod_ABS
- LPMode
- ResetL
- ePPS/Clock.

The TWI signals are the following:

- SCL – clock
- SDA – data.

4.3.1 TxDisable, TxDisableDD

TxDisable and TxDisableDD are module input signals. When TxDisable or TxDisableDD are asserted high or left open, the appropriate SFP-DD/SFP-DD112 module transmitter output shall be turned off unless the module is a passive cable assembly in which case this signal may be ignored. This signal shall be pulled up to VccT in modules and cable assemblies. When TxDisable or TxDisableDD are asserted low or grounded the module transmitter is operating normally.

4.3.2 RxLOS, RxLOSDD

RxLOS (Rx Loss of Signal) and RxLOSDD are open drain/collector outputs that require a resistive pull up to Vcc_Host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 5. When high it indicates an optical signal level below that specified in the relevant standard.

LOS may be an optional function depending on the supported standard. If the LOS function is not implemented, or is reported via the TWI only, the RxLOS contact shall be held low by the module and may be connected to GND within the module.

RxLOS, RxLOSDD assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of LOS a minimum hysteresis of 0.5 dBo is recommended.

4.3.3 Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module inputs and are pulled low to GND with >30 kΩ resistors in the module. Speed1 optionally selects the optical receive signaling rate for channel 1. Speed1DD optionally selects the optical receive signaling rate for channel 2. Speed2 optionally selects the optical transmit signaling rate for the channel 1. Speed2DD optionally selects the optical transmit signaling rate for channel 2. For logical definitions of hardware rate selects Speed1, Speed2, Speed1DD, Speed2DD, see 4.9.

Note: At 128 GFC the FC LSN no longer require to use Speed1, Speed2, Speed1DD and Speed2DD, it is under consideration to reclaim these signals for programmable or other functions.

4.3.4 TxFault

TxFault is a module wide (channel 1 and channel 2) output signal that when high, indicates that the module has detected a fault condition and has entered the Fault state. TxFault signal can optionally be configured as classic SFP Module (channel 1) Fault Indication via TWI as described in the SFP-DD MIS. If TxFault is not

implemented, the contact signal shall be held low by the module and may be connected to GND within the module. The TxFault output is open drain/collector and shall be pulled up to the Vcc_Host on the host board with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 5.

4.3.5 IntL/TxFaultDD

IntL/TxFaultDD is an open collector output that optionally can be configured for either the IntL signal or the TxFaultDD signal. It shall be pulled to Vcc Host on the host board with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 5. At power-up or after ResetL is released to high, IntL/TxFaultDD is configured as IntL. If supported IntL/TxFaultDD can be optionally programmed as TxFaultDD using TWI as defined in the SFP-DD Management Interface Specification.

When IntL/TxFaultDD is configured as IntL, a Low indicates a change in module state, a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using TWI. The IntL signal is de-asserted High after all set flags are read.

When IntL/TxFaultDD is configured as TxFaultDD, a High indicates that the module has detected a fault condition in lane 1 and has entered the Fault state. (See SFP-DD MIS section 6.3.1.11) and if TxFaultDD is not implemented, the contact signal shall be held low by the module.

4.3.6 Mod_ABS

Mod_ABS must be pulled up to Vcc Host on the host board and pulled low in the module. The Mod_ABS is asserted “Low” when the module is inserted. The Mod_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

4.3.7 LPMode

LPMode is an input signal from the host operating with active high logic. The LPMode signal must be pulled up to Vcc in the SFP-DD/SFP-DD112 module. The LPMode signal allows the host to define whether the SFP-DD/SFP-DD112 module will remain in Low Power Mode until software enables the transition to High Power Mode as defined in the SFP-DD management specification. In Low Power Mode (LPMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

4.3.8 ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 7) initiates a complete module reset, returning all user module settings to their default state.

4.3.9 ePPS/Clock PTP Reference Clock (Optional)

Host ePPS/Clock The ePPS/Clock input is a programable timing and clock input, that can support unmodulated 1PPS (1 pulse per second), modulated (1PPS), and reference clock. The ePPS/clock is a LVCMOS compatible signal with series termination (TBD) on the host board and a parallel termination of at least 4.7 kΩ in the module. To improve signal integrity for faster clocks (i.e., 156.25 MHz) the parallel termination can be reduced to as low as 470 Ω and optionally AC coupled.

For high-performance Precision Time Protocol (PTP) applications [15], the ePPS (Enhanced Pulse Per Second) reference either with 1PPS modulated or unmodulated may be provided from the host to the module for time synchronization, see Table 2 for advertise capability. This can be used for either offline delay characterization or real-time delay compensation within the module. The ePPS is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter.

The ePPS/Clock module input optionally can be configured to provide reference clock to the CDR/DSP, see Table 2 for advertise capability.

Table 2- ePPS/Clock Advertising Capabilities

CMIS Byte Location (TBD)	Bit	Mode Supported
xxxxxx--	00	ePPS/Clock not supported
xxxxxx--	01	ePPS/Clock module supports either 1PPS mode, modulated 1PPS, or clock input for encoding see Table 3
xxxxxx--	10	ePPS/Clock supported TOD (Time of Day)
xxxxxx--	11	ePPS/Clock - Reserved

Table 3- ePPS or Clock Modes

CMIS Byte Location (TBD)	Bit	Mode Supported
xxxx--xx	00	RF clock for frequency see table y
xxxx--xx	01	1PPS send as unmodulated pulse duration TBD
xxxx--xx	10	1PPS send as 75%/25% duty cycle on RF modulated clock, for clock frequency see Table 4
xxxx--xx	11	ePPS/Clock - Reserved

Table 4- ePPS or Clock Frequency

CMIS Byte Location (TBD)	Bit	Mode Supported
----xxxx	0000	10 MHz
----xxxx	0001	12.5 MHz
----xxxx	0010	20 MHz
----xxxx	0011	24.576 MHz
----xxxx	0100	25 MHz
----xxxx	0101	156.25 MHz
----xxxx	0110-1101	Reserved
----xxxx	1110-1111	Custom

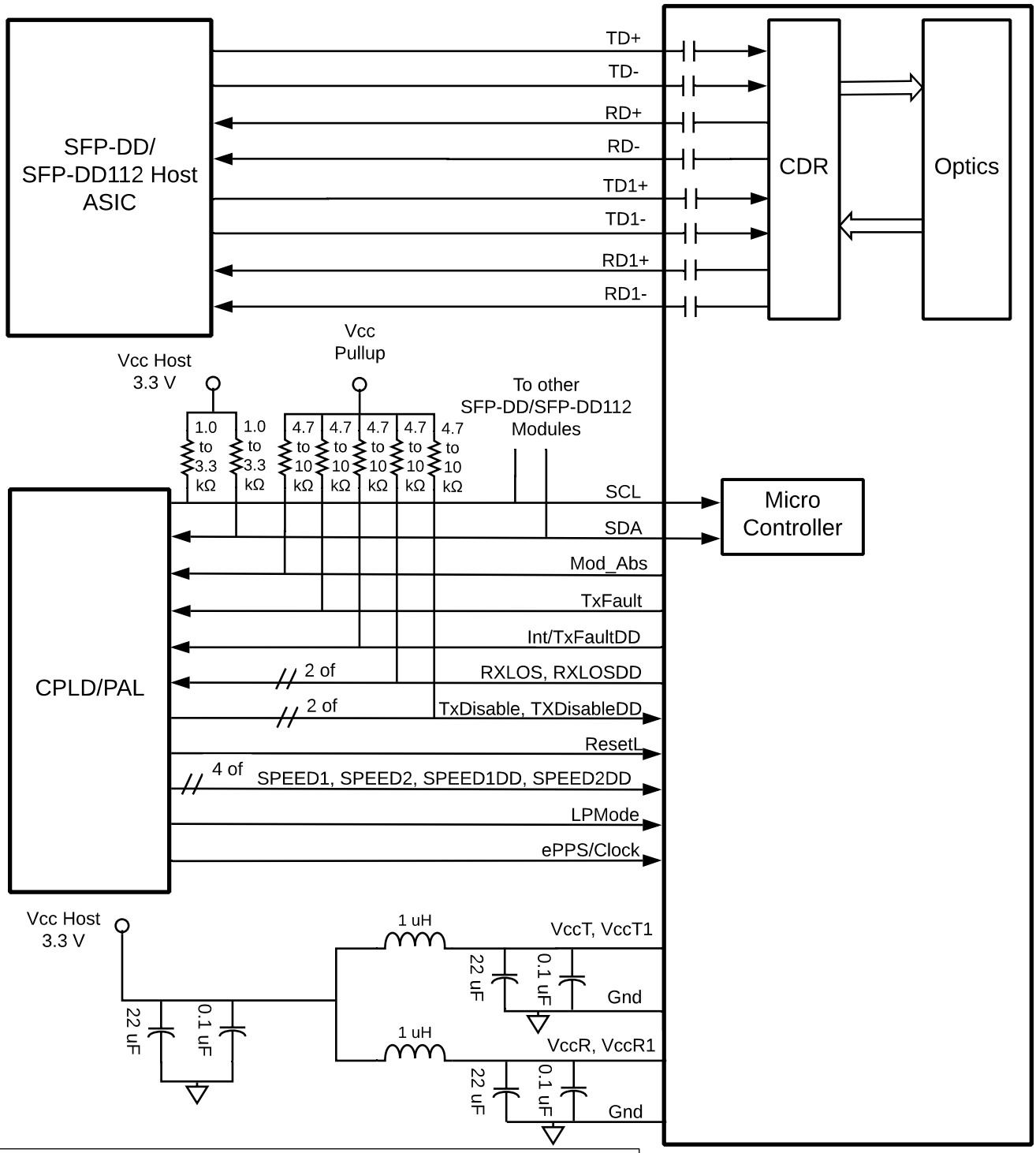
Editor's Note: registers to support optional ePPS/Clock will be added in future revisions of CMIS.

4.3.10 TWI Signals SCL, SDA

SCL is the TWI clock and SDA is the TWI data line. SCL and SDA are pulled up to Vcc_Host by resistors on the host board. For TWI electrical specifications see 4.5.1 and for TWI protocol and timing specifications see Figure 8.

4.4 Example SFP-DD/SFP-DD112 Host Board Schematics

Figure 4, Figure 5 and Figure 6 show examples of SFP-DD/SFP-DD112 host PCB schematics with connections to CDR and control ICs. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

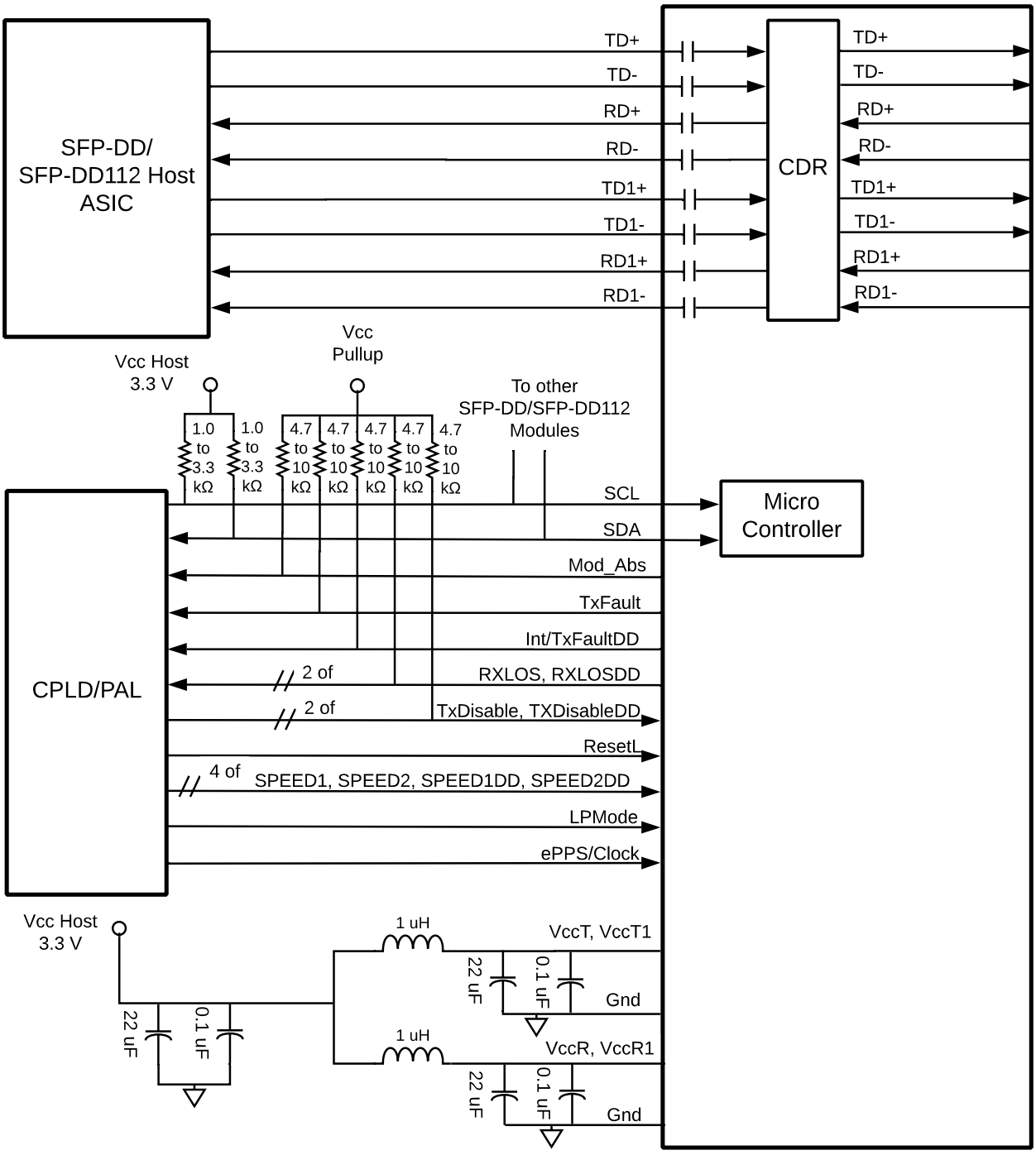


Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.

Note: VccT, VccT1 may be connected to VccR, VccR1 provided the applicable derating of the maximum current limit is used.

SFP-DD/SFP-DD112 Optical Module

Figure 4: Example SFP-DD/SFP-DD112 Host Board Schematic for Optical Modules

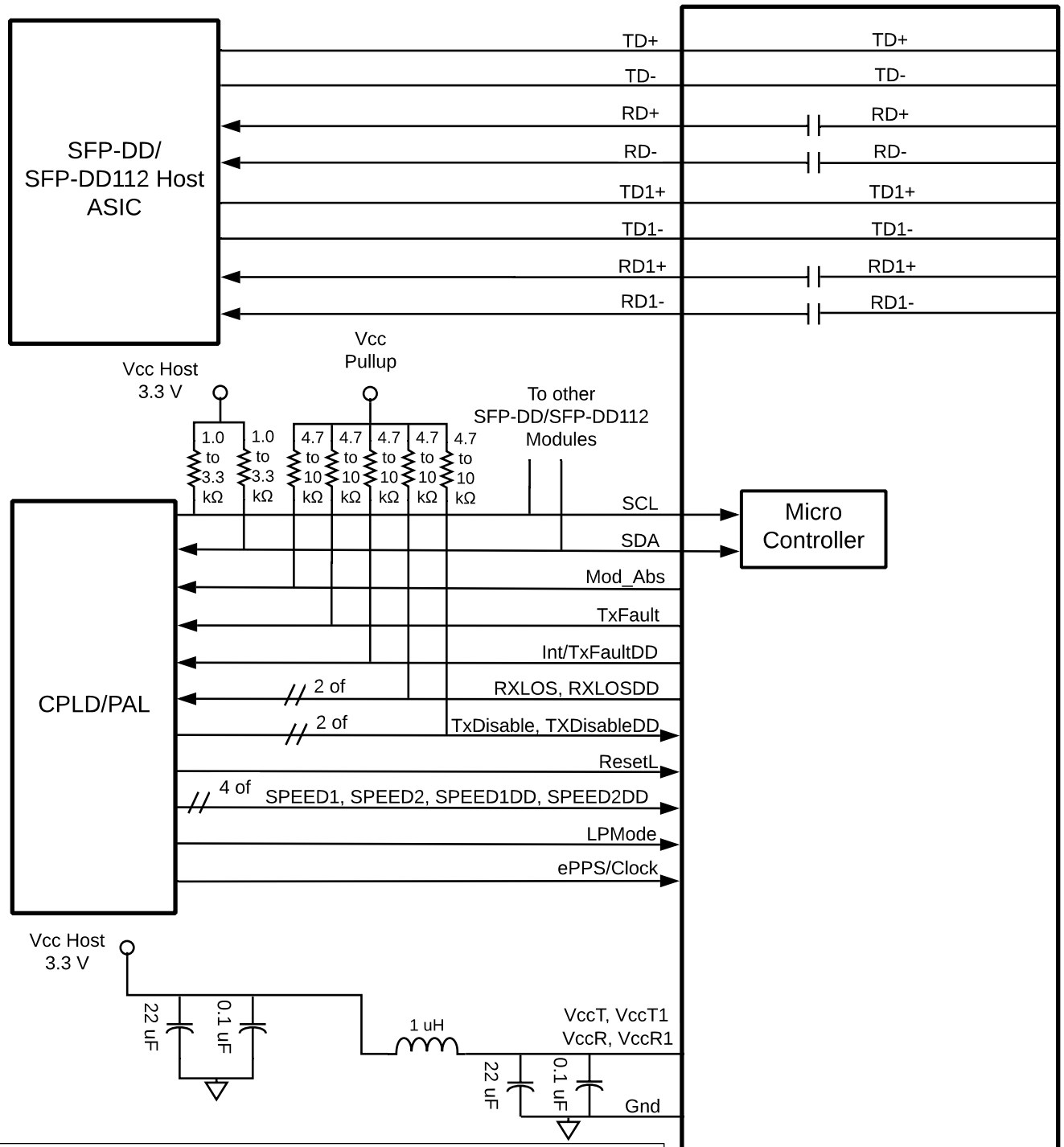


SFP-DD/SFP-DD112
Active Copper Module

Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.

Note: VccT, VccT1 may be connected to VccR, VccR1 provided the applicable derating of the maximum current limit is used.

Figure 5: Example SFP-DD/SFP-DD112 Host Board Schematic for active copper cables



Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.

Note: Recommended filtering is only valid for dedicated passive copper cable ports. For ports supporting both passive and active modules use recommended filtering from Figure 4 and Figure 5.

SFP-DD/SFP-DD112
Passive Copper Module

Figure 6: Example SFP-DD/SFP-DD112 Host Board Schematic for passive copper cables

4.5 Low Speed Electrical Specification

Low Electrical requirements for low speed signals TxDisable, TxDisableDD, RxLOS, RxLOSDD, Speed1, Speed2, Speed1DD, Speed2DD, TxFault, IntL/TXFaultDD, Mod_ABS, LPMode, ResetL and ePPS are based on Low Voltage TTL (LVTTL) [17] operating at a module supply voltage Vcc of 3.3V +/- 5% and with a host supply voltage Vcc_Host range of 2.38 to 3.46V. Vcc is used as a generic term for the supply voltages of VccTx, VccRx, VccPullup or Vcc1. Host biasing requirements (e.g. pullup resistors) are defined in 4.3 and illustrated in 4.4.

Electrical requirements for the TWI signals, SCL and SDA are based on Low Voltage CMOS (LVCMOS) [17] operating at Vcc and compatible with [19]. Host biasing requirements (e.g. pullup resistors) are defined in 4.3 and illustrated in 4.4. Capacitance loading requirements are defined in Table 5 and tradeoffs are illustrated in Figure 7.

4.5.1 TWI Logic Levels and Bus Loading

The SFP-DD/SFP-DD112 low speed electrical specifications are given in Table 5. Implementations compliant to this specification ensures compatibility between host bus initiator and TWI. Tradeoffs among Pull up resistor values, bus capacitance and rise time are shown in Figure 7.

Table 5- Low Speed Control and Sense Signals

Parameters	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	open-drain or open-collector at 3 mA sink current: VDD > 2 V, IOL=3.0 mA for fast mode, 20 mA for fast mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 kΩ Pullup resistor, max. For 1000 kHz clock rate refer to Figure 7.
			200	pF	For 400 kHz clock rate use 1.6 kΩ pullup resistor max. For 1000 kHz clock rate refer to Figure 7.
TxDisable(DD), ResetL, LPMode, Speed(n) and ePPS	VIL	-0.3	0.8	V	For 0V<Vin<Vcc
	VIH	2	Vcc+0.3	V	
LPMode, ResetL, TxDisable(DD), Speed(n)	|Iin|		360	μA	
ePPS	|Iin|		6.5	mA	
Mod_ABS	VOL	0	0.4	V	IOL=2.0 mA, Mod_ABS can be implemented as a short-circuit to GND on the module
RxLOS(DD), TxFault(DD)	VOL	-0.3	0.40	V	4.7 kΩ Pullup resistor to Vcc_Host where Vcc_Host_min<Vcc_Host<Vcc_Host_max
	IOH	-50	37.5	uA	
IntL	VOL	0	0.4	V	IOL = 2.0 mA

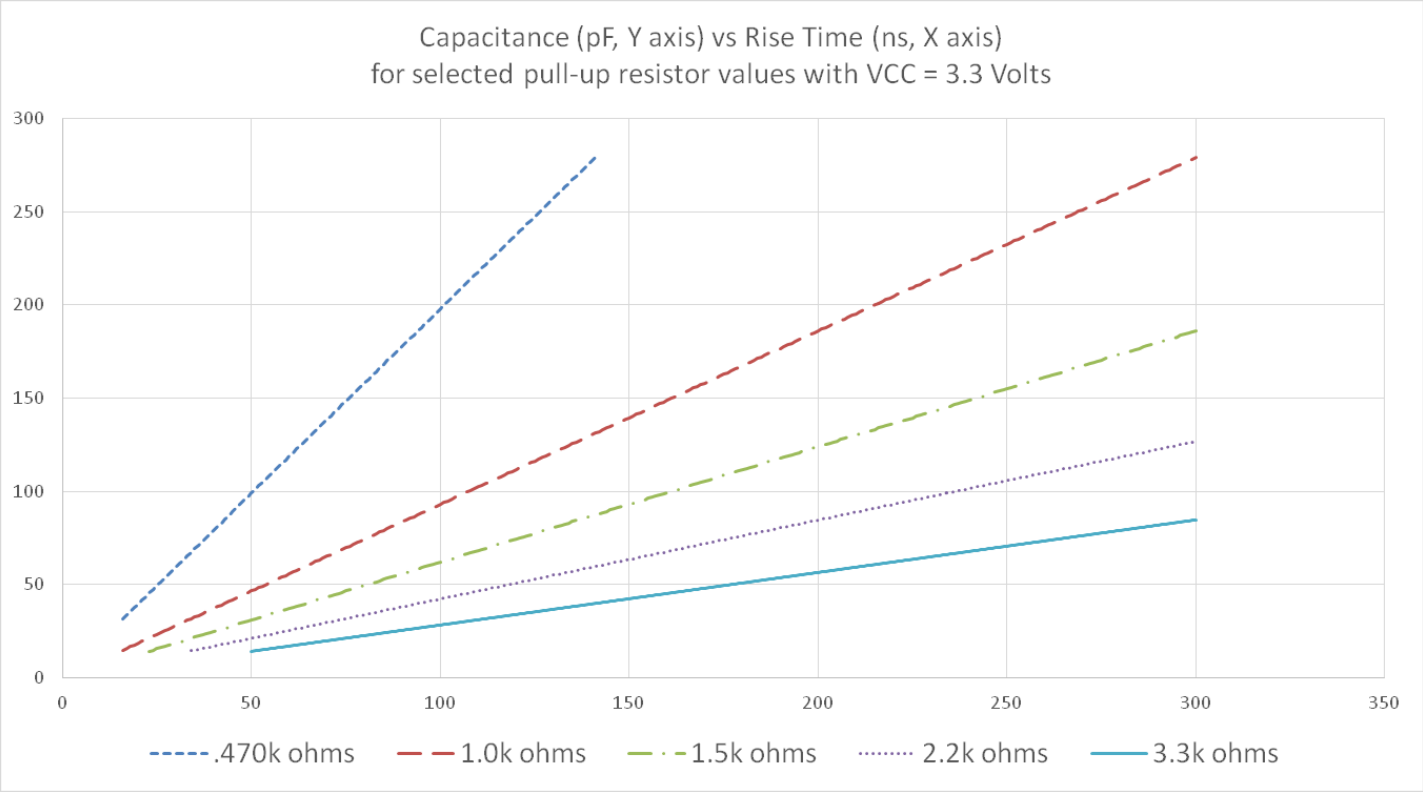


Figure 7: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

4.6 Management Interface and Timing

A management memory interface (See SFP-DD MIS [21], CMIS[5]), as already commonly used in other form factors like QSFP-DD, QSFP, and SFP+ enables module functionality and flexibility beyond that supported by the dedicated hardware signals. Read/Write functionality and protocols are defined in SFP-8419 [29].

Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to advertise the use of the CMIS [5] for SFP-DD112 or MIS [21]. When a classic SFP+/SFP28 module is inserted into an SFP-DD/SFP-DD112 port the host must use the SFP+ memory map, i.e., SFF-8472 [33]. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

Timing requirements for the TWI signals, SCL and SDA are compatible with NXP I2C-bus specifications [19].

Editor Note: It is anticipated that SFP-DD112 management is targeted to use future revisions of CMIS that supports FC.

4.6.1 Management Timing Specification

The SFP-DD/SFP-DD112 TWI and memory management timing illustrated in in Figure 8 and the parameters given in Table 6. Implementations compliant to these specifications ensure compatibility between host bus initiator and the TWI.

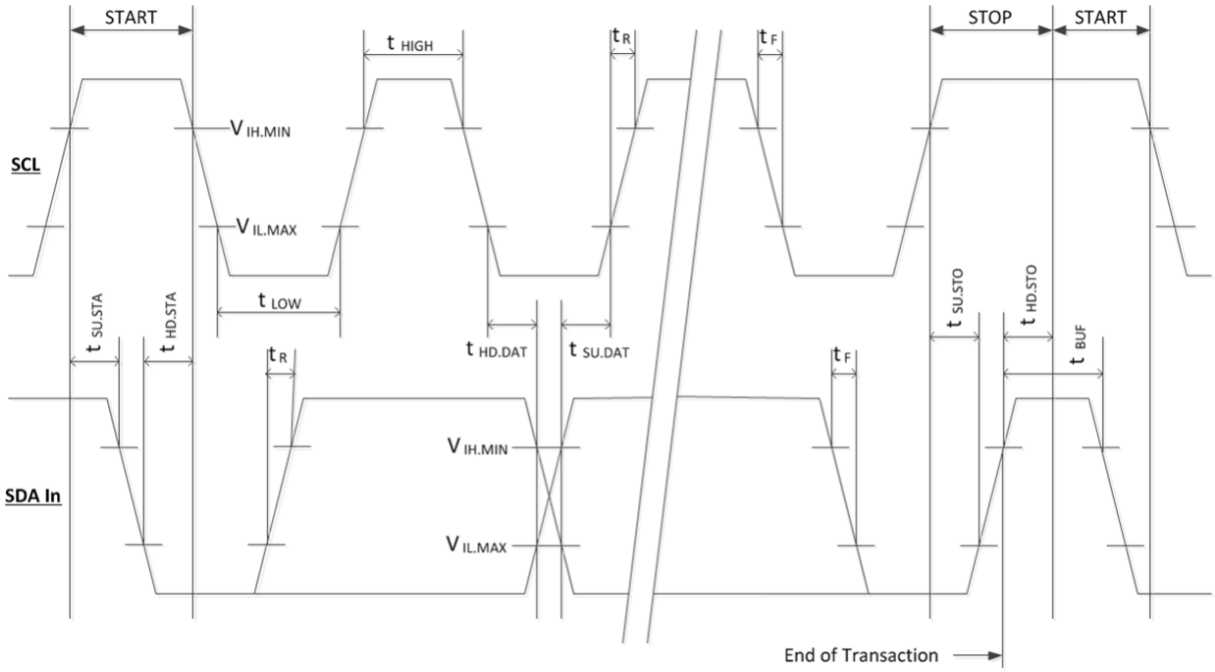


Figure 8: SFP-DD/SFP-DD112 Two Wire Interface Timing

Table 6- Management Interface timing parameters

Parameters	Symbol	Min	Max	Min	Max	Unit	Conditions
		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	t_R		300		120	ns	From (VIL, MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	t_F		300		120	ns	From (VIH, MIN=0.7*Vcc) to (VIL, MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	µs	Maximum time the SFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		80		80	ms	Complete (up to) 8 Byte Write
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50K		50k		cycles	Module Case Temperature = 70 ^oC

4.7 Timing for soft control and status functions

Timing for SFP-DD/SFP-DD112 soft control and status functions are described in Table 7. Squelch and disable timings are defined in Table 8.

Table 7- Timing for SFP-DD/SFP-DD112 soft control and status functions

Parameters	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1] to hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, TXFault and other flag bits.
Rx LOS Assert Time	ton_los		200	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b), LOS signal asserted and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and LOS signal asserted IntL asserted.
TXFault Assert Time	ton_TxFault		200	ms	Time from TXFault state to TXFault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
DataPathDeinit Max Duration	DataPathDeinit_MaxDuration				See SFP-DD MIS Table 7-39 or CMIS memory P01h: B144
DataPathInit Max Duration	DataPathInit_MaxDuration				See SFP-DD MIS Table 7-39 or CMIS memory P01h: B144
Module Pwr Up Max Duration[6]	ModulePwrUp_MaxDuration				See SFP-DD MIS Table 7-48 or CMIS memory P01h: B167
ModulePwrDn Max Duration	ModulePwrDn_MaxDuration				See SFP-DD MIS Table 7-48 or CMIS memory P01h: B167
Data Path TX Turn On Max Duration	DataPathTxTurnOn_MaxDuration				See SFP-DD MIS Table 7-48 or CMIS memory P01h: B168
Data Path TX Turn Off Max Duration	DataPathTxTurnOff_MaxDuration				See SFP-DD MIS Table 7-48 or CMIS memory P01h: B168

Notes:
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 12.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Measured from low to high SDA edge of the Stop condition of the write transaction.
4. Rx LOS condition is defined at the optical input by the relevant standard.

Table 8- I/O Timing for Squelch & Disable

Parameters	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	100	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 4.8.1.
Rx Squelch Deassert Time	toff_Rxsq	10	s	Time from resumption of Rx input signals until normal Rx output condition is reached, see 4.8.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 4.8.2.
Tx Squelch Deassert Time	toff_Txsq	10	s	Time from resumption of Tx input signals until normal Tx output condition is reached, see 4.8.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence [1] until optical output falls below 10% of nominal, see note 2 and 3.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal, see note 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 2 and 3.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Notes:
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in CMIS or SFP-DD MIS P01h.168.
3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (CMIS or SFP-DD MIS P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

4.8 High Speed Electrical Specifications

For detailed electrical specifications see the appropriate specification, e.g. IEEE Std 802.3-2018 [12]; IEEE Std 802.3cd [13], 802.3ck [14]; FC-PI-6 [1], FC-PI-7[2], FC-PI-8 [3]; OIF-CEI-4.0 [20], or the InfiniBand specifications [16].

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations given in clause 4.8.1 and 4.8.2 may be used.

4.8.1 RD0+, RD0-, RD1+, RD1-

RD(n)+/- are SFP-DD/SFP-DD112 module receiver data outputs. Rx(n)+/- are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the SFP-DD/SFP-DD112 module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.
Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to

assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Table 24. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

4.8.2 TD0+, TD0-, TD1+, TD1-

TD(n)+/- are SFP-DD/SFP-DD112 module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the SFP-DD/SFP-DD112 optical module. The AC coupling is implemented inside the SFP-DD/SFP-DD112 optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input lane becoming less than the TX Squelch Levels specified in Table 9 when terminated in to 100 Ω differential, then the transmitter optical output associated with that electrical input lane shall be squelched and the associated TxLOS flag set. If multiple electrical input lanes are associated with the same optical output lane, the loss of any of the incoming electrical input lanes causes the optical output lane to be squelched.

Table 9- TX Squelch Levels

Data Rate	Levels	Unit
OIF 28G-VSR/IEEE 802.3 CL83E	70	mV [1]
OIF 56G-VSR/IEEE 802.3 CL120E	70	mV [1]
OIF 112G-VSR/IEEE 802.3 CL120G	50	mV [1]
1. Differential peak-peak.		

For applications, e.g., Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where TX Squelch is implemented, the default case has TX Squelch active. TX Squelch can be deactivated using TX Squelch Disable through the 2-wire serial interface. TX Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

4.9 Rate Select Hardware Control

The module provides 4 inputs Speed1, Speed2, Speed1DD and Speed2DD that can optionally be used for rate selection as defined in Table 10. Speed1, Speed1DD specifies the highest rate advertised by the channels. Speed2, Speed2DD specifies a lower speed for each channel. Speed1 controls the receive path signaling rate capability for the channel 1 receive path. Speed1DD controls the receive path signaling rate capability for the channel 2 receive path. Similarly, Speed2 controls the transmit path signaling rate capability for channel 1 and Speed2DD controls the transmit path signaling rate capability for the channel 2 transmit path.

The rate select functionality can also be controlled by software as defined by the SFP-DD or SFP-DD112 management specification.

For 64 GFC FC-PI-8 [3] operation link speed is determined with FC Link Speed Negotiation (LSN) exchange while the link is operating at 32 GFC.

Table 10- Rate Select Hardware Control

Parameters	**State**	**Conditions**

Speed1, Speed1DD	Low	RX signaling rate of 14.025 GBd (16 GFC)[1]
	High	RX signaling rate of 28.05 GBd (32 GFC)
Speed2, Speed2DD	Low	TX signaling rate of 14.025 GBd (16 GFC) [1]
	High	TX signaling rate of 28.05 GBd (32 GFC)
Note 1: For SFP-DD112 operating at 128 GFC there is no requirement for 16 GFC or rate select.		

4.10 Power Requirements

SFP-DD/SFP-DD112 has four designated power supply pins VccT, VccT1 VccR, VccR1 in the connector. Power is applied concurrently to VccT, VccR in the row for channel 1 and concurrently to VccT1, VccR1 in the row for channel 2.

A host board together with the SFP-DD/SFP-DD112 module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 12 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.10.1 Power Classes and Maximum Power Consumption

SFP-DD/SFP-DD112 power classes are defined in Table 11. Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host identify the power class of the module before allowing the module to go into high power mode.

Power levels associated with classifications of modules are shown in Table 11.

Table 11- Power Classification

Power Class	Max Power (W)
1	1.0
2	1.5
3	2.0
4	3.5
5	5.0
6	reserved
7	reserved
8	See management register for maximum power consumption.

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.10.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 9.

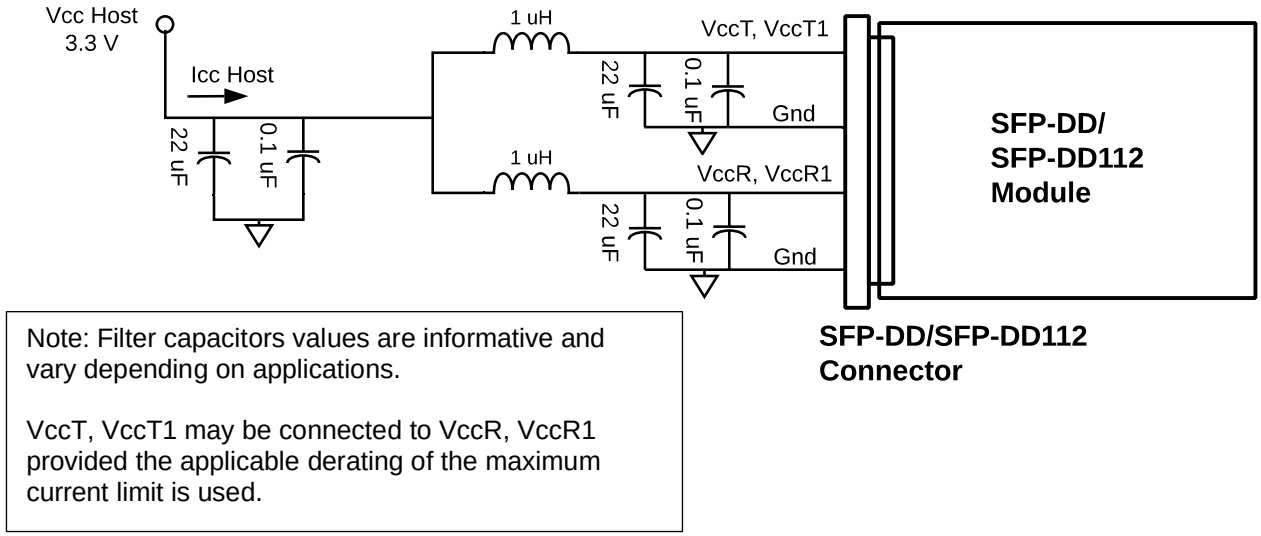


Figure 9: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 μF capacitors each have an equivalent series resistance of 0.22 ohms.

The specifications for the power supply are shown in Table 12. The limits in Table 12 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 24). An example test method for measuring inrush current can is Keysight Technologies application brief 5991-2778EN.pdf.

4.10.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all SFP-DD/SFP-DD112 modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 10 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 12.

Table 12- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1 including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Low Power Mode[2]					
Power Consumption	P_lp		.5		W
Instantaneous peak current at hot plug	Icc_ip_lp	-	200		mA
Sustained peak current at hot plug	Icc_sp_lp	-	165		mA
Steady state current	Icc_lp	See Note 4			mA
High Power Class 1 module					
Power Consumption	P_1		1.0		W
Instantaneous peak current	Icc_ip_1	-	400		mA
Sustained peak current	Icc_sp_1	-	330		mA
Steady state current	Icc_1	See Note 4			mA
High Power Class 2 module					
Power Consumption	P_2		1.5		W
Instantaneous peak current	Icc_ip_2	-	600		mA
Sustained peak current	Icc_sp_2	-	495		mA
Steady state current	Icc_2	See Note 4			mA
High Power Class 3 module					
Power Consumption	P_3		2.0		W
Instantaneous peak current	Icc_ip_3	-	800		mA
Sustained peak current	Icc_sp_3	-	660		mA
Steady state current	Icc_3	See Note 4			mA
High Power Class 4 module					
Power Consumption	P_4		3.5		W
Instantaneous peak current	Icc_ip_4	-	1400		mA
Sustained peak current	Icc_sp_4	-	1155		mA
Steady state current	Icc_4	See Note 4			mA
High Power Class 5 module					
Power Consumption	P_5		5.0		W
Instantaneous peak current	Icc_ip_5	-	2000		mA
Sustained peak current	Icc_sp_5	-	1650		mA
Steady state current	Icc_5	See Note 4			mA
High Power Class 8 module					
Power Consumption	P_8[3]				W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	4	A

Notes:
1. Measured at VccT, VccR, VccT1, and VccR1.
2. Host designers are responsible for handling 1.5W Low Power Mode SFP(INF-8074i)/SFP+(SFF-8431) classic modules as appropriate in their system.
3. User must read management register for maximum power consumption.
4. The module must stay within its declared power class.

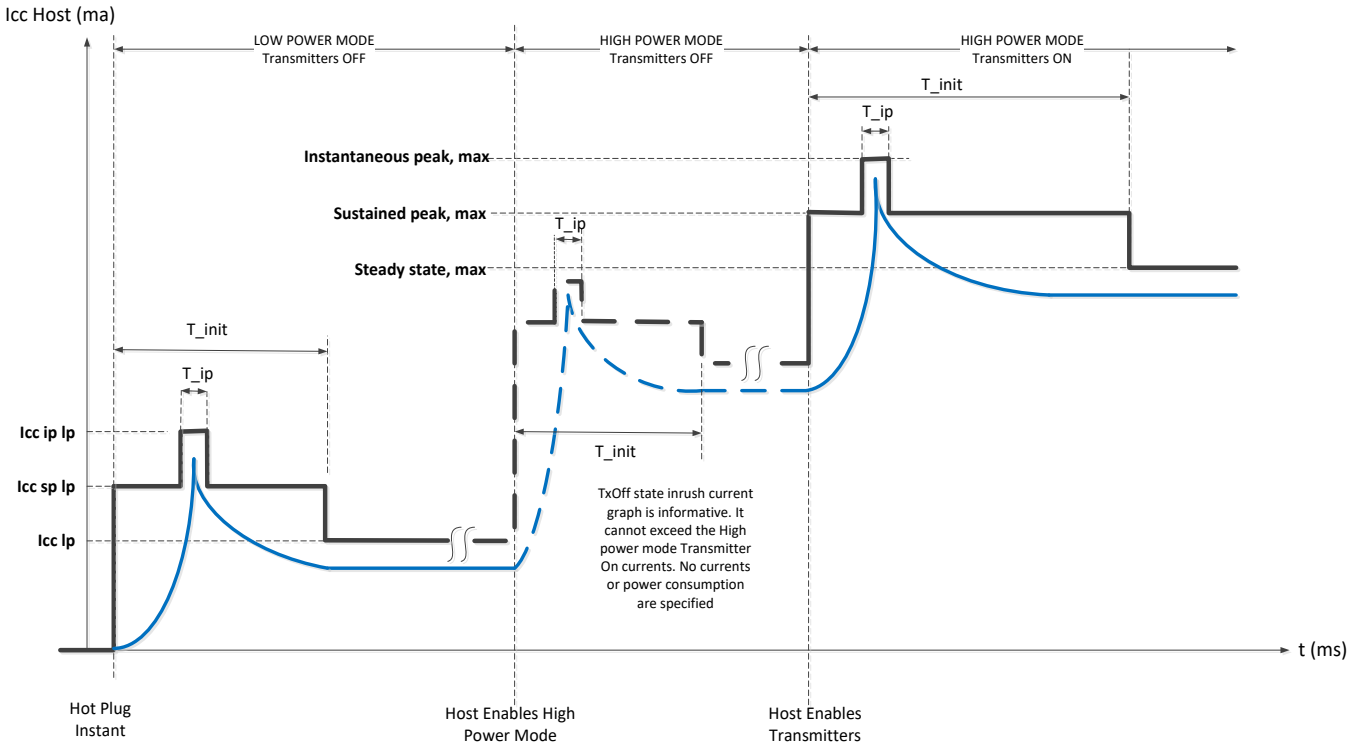


Figure 10: Instantaneous and sustained peak currents for Icc Host (see Table 12)

4.10.4 Host Board Power Supply Noise Output

The host noise output on VccT/VccT1, and VccR/VccR1 supplies are defined with resistive loads that draws the maximum rated power supported by the host power class, see Figure 11. The resistive loads are connected in place of the module between VccT/VccT1 and VccR/VccR1 and the Vee. When the noise is measured on VccT/VccT1, VccR/VccR1 is left open circuit, and vice versa. Host power supply limits are given in Table 11. The noise power spectrum is measured for each of the 2 rails then integrated from 40 Hz to 10 MHz and converted to a voltage, eN_Host, with limit specified in Table 13.

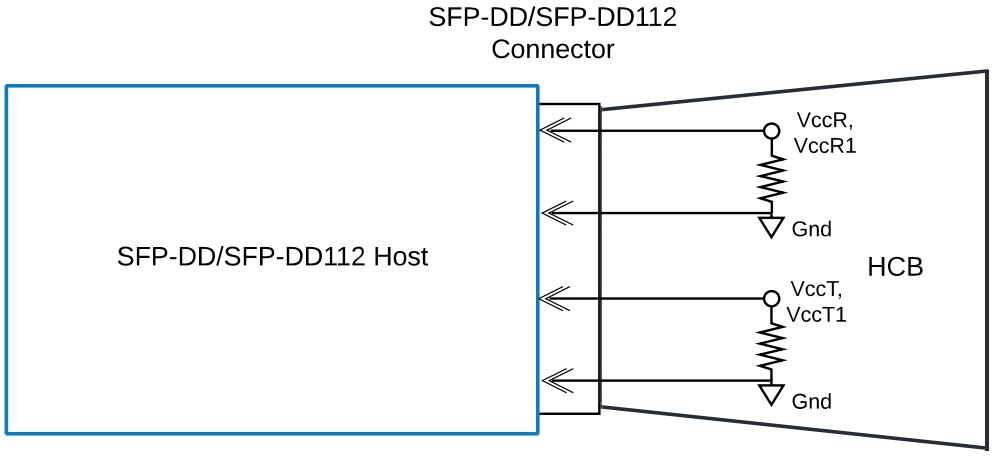


Figure 11: Host Noise Output Measurement

4.10.5 Module Power Supply Noise Output

The SFP-DD/SFP-DD112 modules, when plugged into a reference module compliance board shall generate noise less than the value in Table 13. The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from in- side the module back onto the host board. A power meter technique, or a spectrum analyzer technique with integration of the spectrum, may be used.

The RMS module noise voltage output is defined in the frequency band from 40 Hz to 10 MHz. Module noise output shall be measured with an appropriate probing technique at point X, Figure 12 and must meet limits given in Table 13. The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

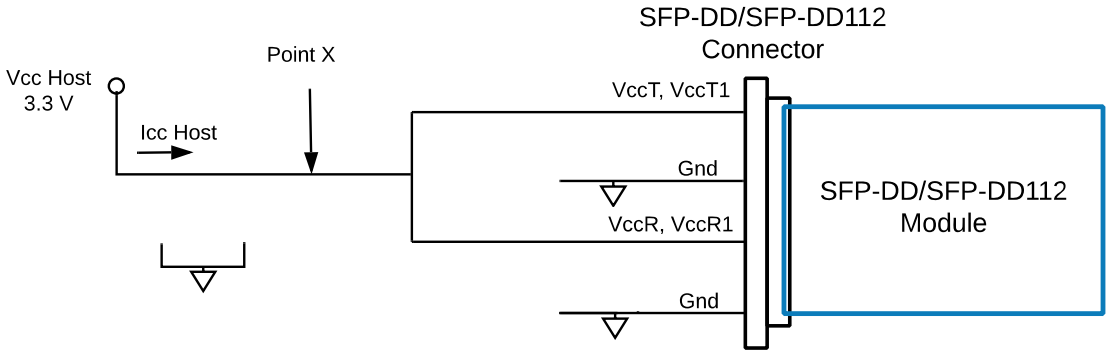


Figure 12: Module Noise Output Measurement

4.10.6 Module Power Supply Noise Tolerance

The SFP-DD/SFP-DD112 modules shall meet all requirements and operate within the design specifications in the presence of a reference noise waveform described in Table 13 superimposed on the DC voltage. The reference noise waveform consists of a sinusoidal 40 Hz to 10 MHz noise generated by Osc1 and added to Vcc PSU, see Figure 13. This emulates the worst-case noise that the module must tolerate and operate within the design specifications. The reference noise is generated by Osc1 and amplified by the Power OpAmp then added to Vcc PSU through a Bias-T, see Figure 10. Example of suitable Power OpAmp are Analog Devices ADA4870 and TI THS3491. With power supply filter components removed, point X measures the noise voltage applied to the module. To facilitate power supply tolerance testing at frequencies < ~100 kHz due to Power OpAmp interaction with PSU and low frequency response of the Bias-T, it is recommended to use noise source Osc2 modulating PSU sense line to generate sinusoidal noise directly on the PSU output, see Figure 14. Osc2 amplitude level is adjusted while observing point X amplitude level as defined in Table 13 for module in low power and high-power modes. To modulate the PSU sense lines, the PSU must have high speed sense tracking. An example of PSU with high-speed sense tracking are TI TPSM5D1806 and Keysight N6700 with N6781/N6782 plugins.

For modules without or limited input stage power filtering one may measure the applied noise to the module by measuring point X directly while the module is active and either in low or high-power modes. But to take credit for any input stage power filtering in the module, the DUT module is replaced with a resistive load drawing equivalent current of a module configured in low power mode, the DUT module is then replaced with a resistive load drawing equivalent current of a module configured in high power mode. Osc1 and Osc2 are adjusted to produce maximum PSNR level as defined in Table 13 at point X with resistive loads drawing the same power as the module in low and high-power modes. The resistive loads are then replaced with the DUT module with the same Osc1/Osc2 amplitude settings that produced the max PSNR with the resistive loads.

Notes: An appropriate probing technique is required for noise measurement at point X. For modules with limited or no decoupling directly connected to host PSU, the PSNR can be directly measured at point X with module plugged into the host for module operating in low power and high power modes. Osc1 or Osc2 are adjusted to provide maximum PSNR at point X for a given module in low power and full power modes.

Table 13- Power Supply Output Noise and Tolerance Specifications

Parameter	Symbol	Min	Nom	Max	Unit
Host RMS noise output 40 Hz-10 MHz (eN_Host) [1, 3]				25	mV
Module RMS noise output 40 Hz - 10 MHz [2, 3]				30	mV
Module sinusoidal power supply noise tolerance 40 Hz - 10 MHz (p-p) [2, 3]	$PSNR_{mod}$			66	mV

Notes:
1. Host must be tested for all supported power classes
2. Module must be test at low and high power modes
3. Recommended test frequencies:
   40, 50, 60, 70, 80, 90 Hz
   100, 200, 300, 400, 500, 600, 700, 800, 900 Hz
   1, 2, 3, 4, 5, 6, 7, 8, 9 kHz
   10, 20, 30, 40, 50, 60, 70, 80, 90 kHz
   100, 200, 300, 400, 500, 600, 700, 800, 900 kHz
   1, 2, 3, 4, 5, 6, 7, 8, 9, 10 MHz.

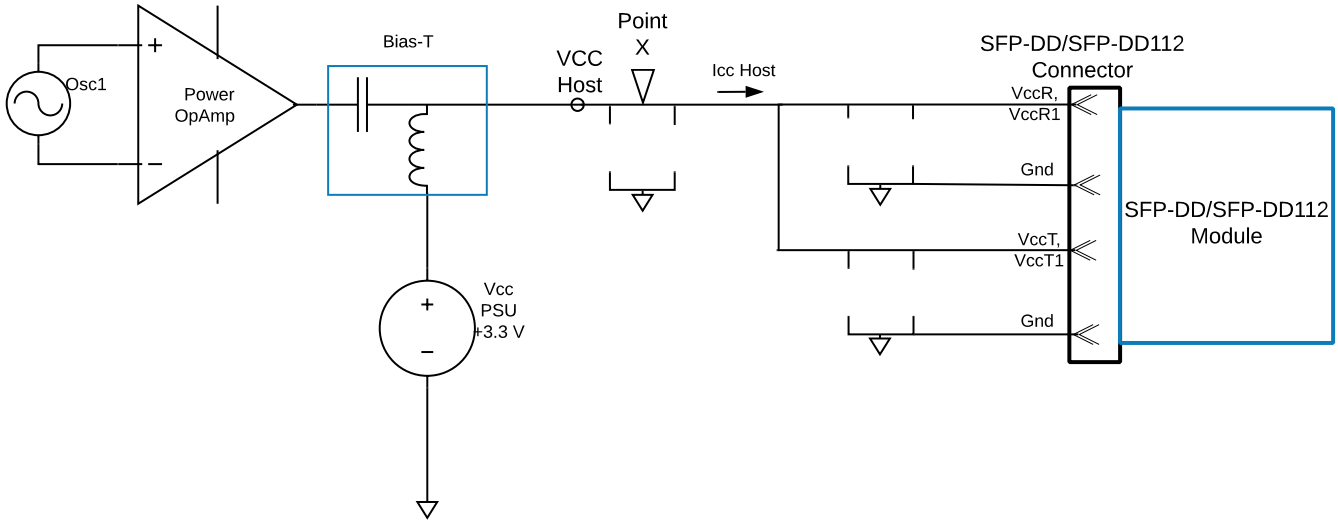


Figure 13: Module High Frequency Noise Tolerance

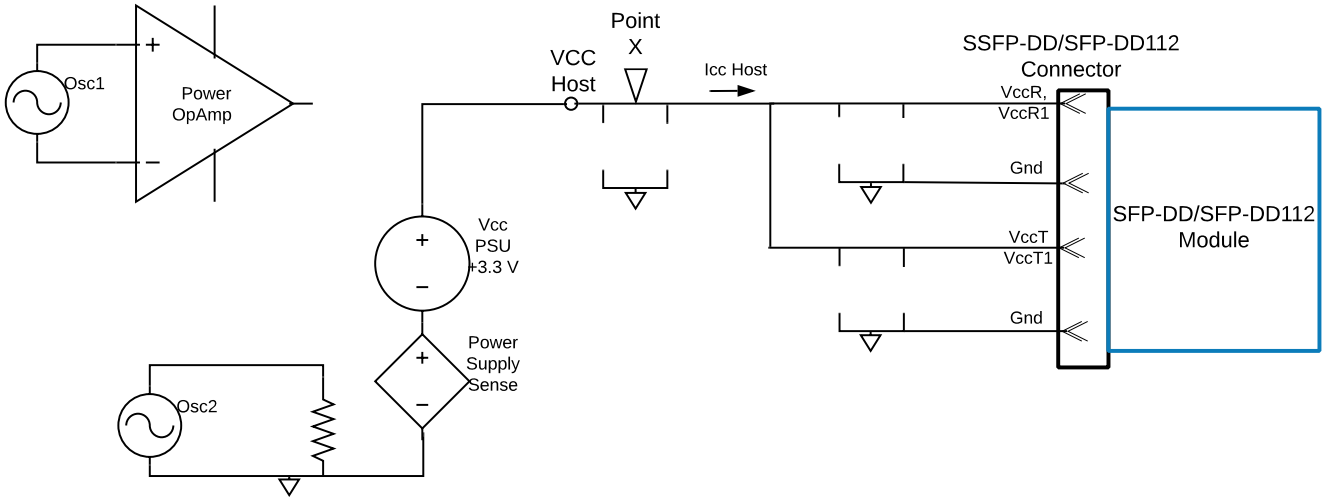


Figure 14: Module Low Frequency Noise Tolerance

4.11 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the SFP-DD/SFP-DD112 module shall meet ESD requirements given in EN61000-4-2 [8], criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case. All the SFP-DD/SFP-DD112 module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001 [9].

5. Electrical Specification and Management Interface Timing for SFP112

This chapter contains signal definitions and requirements that are specific to the SFP112 modules. SFP112 modules are backward compatible with SFP+ [30] and SFP28 [28] modules. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

5.1 General Requirements

The SFP112 modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered.

For EMI protection the signals from the host connector should be shut off when the SFP112 module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines are recommended. The SFP112 module signal ground contacts GND should be isolated from module case. An isolated SFP112 module case from signal ground provides equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground (GND) of the module.

All electrical specifications shall be met over the entire specified range of power supplies given in section 5.10.

5.2 SFP112 Electrical Connector

The SFP112 module edge connector consists of a single paddle card with 10 pads on the top and 10 pads on the bottom of the paddle card for a total of 20 pads compatible with SFF-8071 [27], but improved for 112G operation.

The pads are designed for a sequenced mating:

- First mate – ground pads
- Second mate – power pads
- Third mate – signal pads.

Figure 15 shows the signal symbols and pad numbering for the SFP112 modules edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 20 pads intended for high speed signals, low speed signals, power and ground connections.

Table 14 provides more information about each of the 20 pads. Figure 58 shows SFP112 improved pad dimensions. The surface mount SFP112 SMT connector configuration is shown in Figure 59.

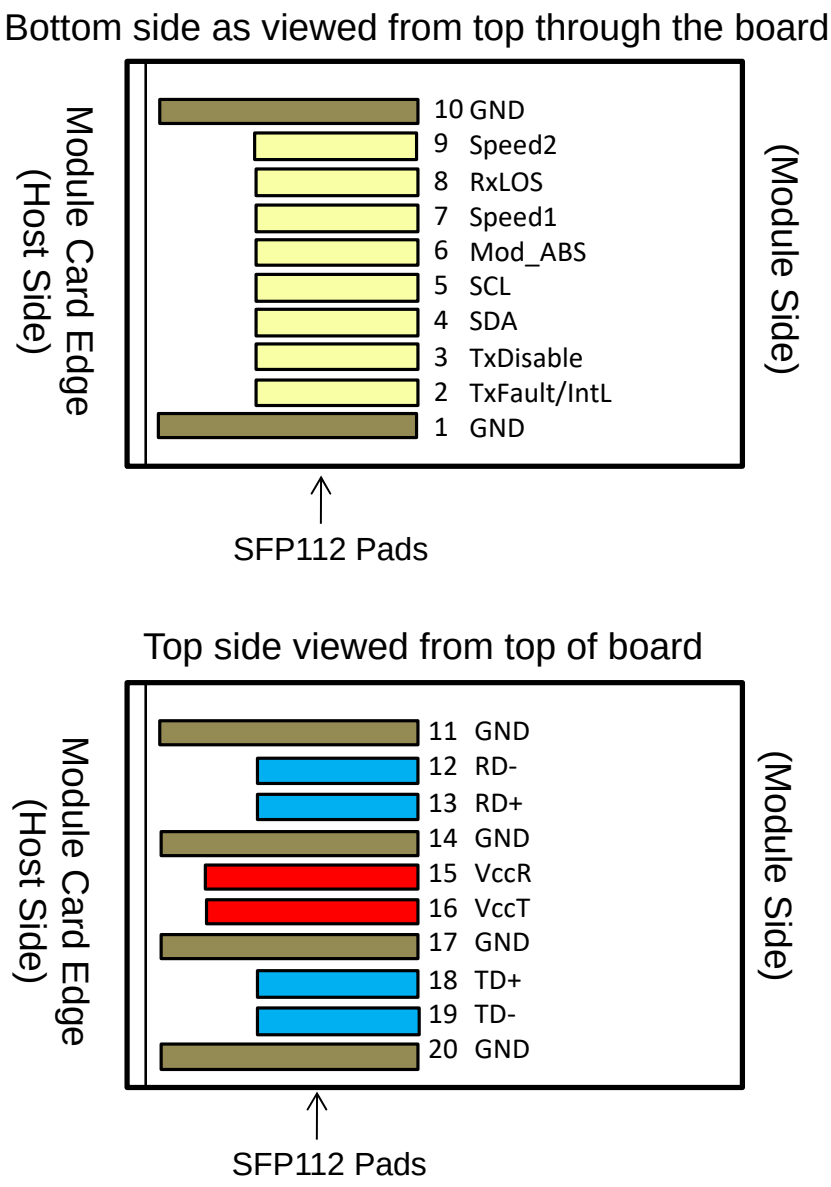


Figure 15: SFP112 module pad layout

SFP112 module pads are compatible with SFP+/SFP28 [30], [28], for list of pad functions see Table 1. For a reliable interconnect, a sufficient contact wipe of the connector pins sliding over the module gold pads is required. In the past, long signal pads have been used to provide the mechanical wipe. As operating speeds were relatively slow, the electrical stub was not an issue with signal integrity.

As operating speeds have increased, signal pad lengths have become shorter and shorter to reduce electrical stubs, however this caused insufficient mechanical wipe. A solution is to add a small passive 'pre-wipe" pad prior to active signal pad.

Table 14- Pad Function Definition

Pad	Logic	Symbol	Module Pad Descriptions	Plug Sequence[3]	Notes
0		Case	Module case	0	
1		GND	Ground	1	1
2	LVTTL-O	TXFault/IntL	Module Fault Indication optionally can be configured IntL via TWI as described in the CMIS	3	4
3	LVTTL-I	TxDisable	Transmitter Disable	3	
4	LVCMOS-I/O	SDA	Management I/F data line	3	
5	LVCMOS-I/O	SCL	Management I/F clock	3	
6	LVTTL-O	Mod_ABS	Module Absent	3	
7	LVTTL-I	Speed1	Rx Rate Select	3	
8	LVTTL-O	RxLOS	Rx Loss of Signal	3	
9	LVTTL-I	Speed2	Tx Rate Select	3	
10		GND	Ground	1	1
11		GND	Ground	1	1
12	CML-O	RD0-	Inverse Received Data Out	3	
13	CML-O	RD0+	Received Data Out	3	
14		GND	Ground	1	1
15		VccR	Receiver Power	2	2
16		VccT	Transmitter Power	2	2
17		GND	Ground	1	1
18	CML-I	TD0+	Transmit Data	3	
19	CML-I	TD0-	Inverse Transmit Data	3	
20		GND	Ground	1	1

Notes:
1. SFP112 uses common ground (GND) for all signals and supply (power). All are common within the SFP112 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccR, VccT shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 21Table 12. VccR and VccT may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 0, 1, 2, 3.
4. Support to configure TXFault/IntL will be provided in future CMIS revisions 5.1+.

5.3 Overview of the Low Speed Electrical Hardware Signals

The SFP112 connector allocates contacts for a set of low speed signals for control, status and management by the host. These include dedicated hardware signals and TWI signals. The dedicated hardware signals are the following:

- TxDisable
- RxLOS
- Speed1, Speed2
- TxFault/IntL
- Mod_ABS.

The TWI signals are the following:

- SCL – clock
- SDA – data.

5.3.1 TxDisable

TxDisable is a module input signals. When TxDisable is asserted high or left open, the appropriate SFP112 module transmitter output shall be turned off unless the module is a passive cable assembly in which case this

signal may be ignored. This signal shall be pulled up to VccT in modules and cable assemblies. When TxDisable is asserted low or grounded the module transmitter is operating normally.

5.3.2 RxLOS

RxLOS (Rx Loss of Signal) is an open drain/collector outputs that require a resistive pull up to Vcc_Host with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according to Table 15. When high it indicates an optical signal level below that specified in the relevant standard.

LOS may be an optional function depending on the supported standard. If the LOS function is not implemented, or is reported via the TWI only, the RxLOS contact shall be held low by the module and may be connected to GND within the module.

RxLOS assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of LOS a minimum hysteresis of 0.5 dBo is recommended.

5.3.3 Speed1, Speed2

Speed1, Speed2 are module inputs and are pulled low to GND with >30 kΩ resistors in the module. Speed1 optionally selects the optical receive signaling rate. Speed2 optionally selects the optical transmit signaling rate for.

5.3.4 TxFault/IntL

TxFault/IntL is an open collector output and shall be pulled to Vcc Host on the host board with a resistor in the range 4.7 kΩ to 10 kΩ, or with an active termination according Table 15.

TxFualt/IntL default setting indicates TxFault, but optionally can be configured as IntL through CMIS. TxFault indicate the module has detected a fault condition and has entered the Fault state. When TxFault/IntL is configured as IntL, a Low indicates a change in module state, a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using TWI. The IntL signal is de-asserted High after all set flags are read.

At power-up or after ResetL is released to high, TxFault/IntL is configured as TxFault. If supported TxFault/IntL can be optionally programmed as IntL using TWI as defined in the CMIS.

5.3.5 Mod_ABS

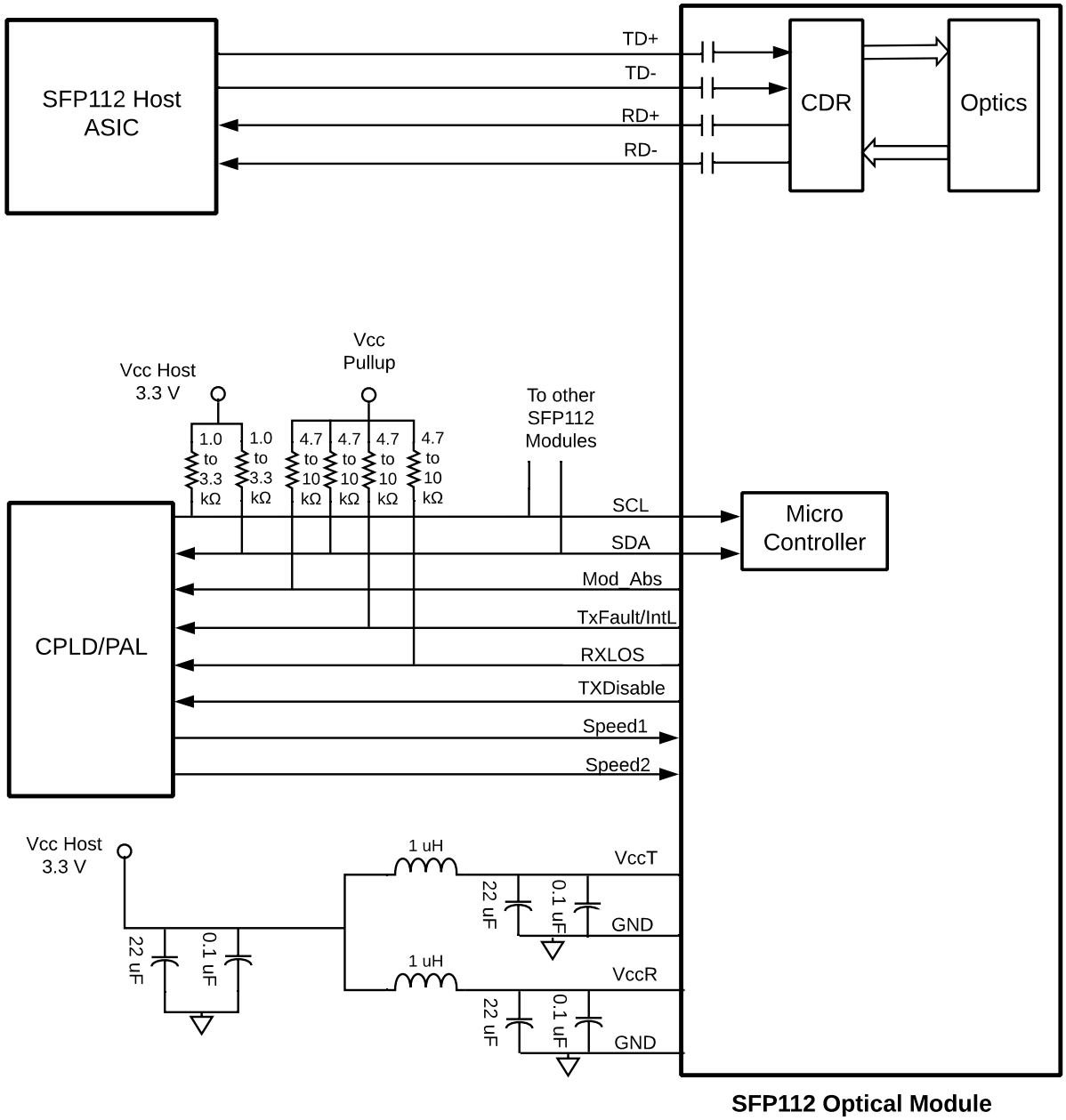
Mod_ABS must be pulled up to Vcc Host on the host board and pulled low in the module. The Mod_ABS is asserted “Low” when the module is inserted. The Mod_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

5.3.6 TWI Signals SCL, SDA

SCL is the TWI clock and SDA is the TWI data line. SCL and SDA are pulled up to Vcc_Host by resistors on the host board. For TWI electrical specifications see 5.5.1 and for TWI protocol and timing specifications see Figure 20.

5.4 Example SFP112 Host Board Schematics

Figure 16, Figure 17, and Figure 18 show examples of SFP112 host PCB schematics with connections to CDR and control ICs. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

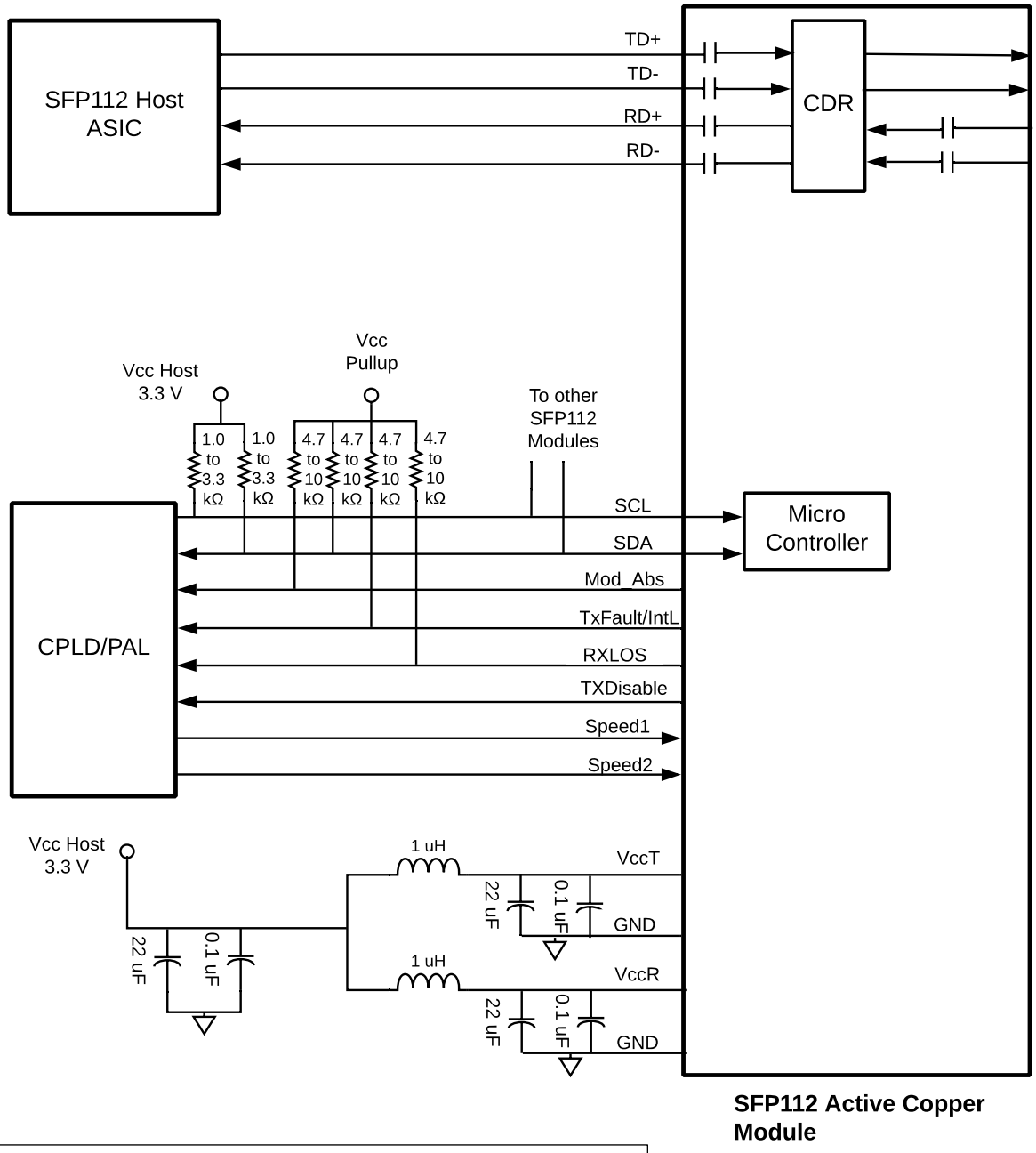


SFP112 Optical Module

Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.

Note: VccT may be connected to VccR provided the applicable derating of the maximum current limit is used.

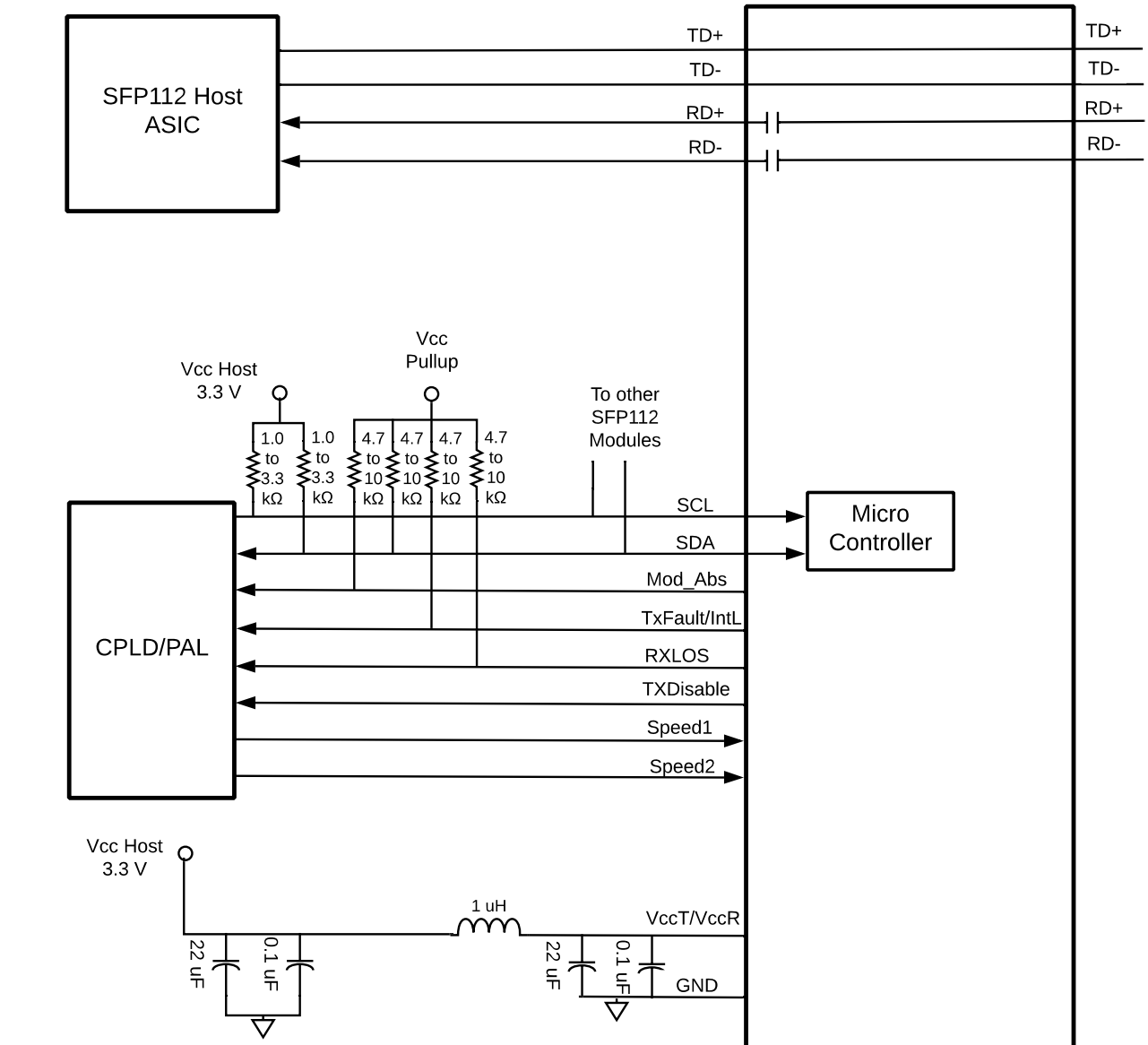
Figure 16: Example of SFP112 Host Board Schematic for Optical Modules



Note: Filter capacitors values are informative and application dependent, 0.1 mF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: VccT may be connected to VccR within the module provided the applicable derating of the maximum current limit is used.

Figure 17: Example of SFP112 Host Board Schematic for active copper cables



Note: Filter capacitors values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.

Note: Recommended filtering is only valid for dedicated passive copper cable ports. For ports supporting both passive and active modules use recommended filtering from Figure 16 or Figure 17.

Figure 18: Example of SFP112 Host Board Schematic for passive copper cables

5.5 Low Speed Electrical Specification

Low Electrical requirements for low speed signals TxDisable, RxLOS, Speed1, Speed2, IntL/TxFault, IntL/TXFaultDD, and Mod_ABS are based on Low Voltage TTL (LVTTL) [17] operating at a module supply voltage Vcc of 3.3V +/- 5% and with a host supply voltage Vcc_Host range of 2.38 to 3.46V. Vcc is used as a generic term for the supply voltages of VccTx, VccRx, or VccPullup. Host biasing requirements (e.g. pullup resistors) are defined in 5.3 and illustrated in 5.4.

Electrical requirements for the TWI signals, SCL and SDA are based on Low Voltage CMOS (LVCMOS) [17] operating at Vcc and compatible with [19]. Host biasing requirements (e.g. pullup resistors) are defined in 5.3 and illustrated in 5.4. Capacitance loading requirements are defined in Table 15 and tradeoffs are illustrated in Figure 19.

5.5.1 TWI Logic Levels and Bus Loading

The SFP112 low speed electrical specifications are given in Table 15. Implementations compliant to this specification ensures compatibility between host bus initiator and TWI. Tradeoffs among Pull up resistor values, bus capacitance and rise time are shown in Figure 19.

Table 15- Low Speed Control and Sense Signals

Parameters	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	open-drain or open-collector at 3 mA sink current: VDD > 2 V, IOL=3.0 mA for fast mode, 20 mA for fast mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 kΩ Pullup resistor, max. For 1000 kHz clock rate refer to Figure 19Figure 7.
			200	pF	For 400 kHz clock rate use 1.6 kΩ pullup resistor max. For 1000 kHz clock rate refer to Figure 19.
TxDisable, Speed1, Speed2	VIL	-0.3	0.8	V	For 0V<Vin<Vcc
	VIH	2	Vcc+0.3	V	
TxDisable, Speed1, Speed2	|Iin|		360	μA	
Mod_ABS	VOL	0	0.4	V	IOL=2.0 mA, Mod_ABS can be implemented as a short-circuit to GND on the module
RxLOS, TxFault/IntL	VOL	-0.3	0.40	V	4.7 kΩ Pullup resistor to Vcc_Host where Vcc_Host_min<Vcc_Host<Vcc_Host_max
	IOH	-50	37.5	uA	

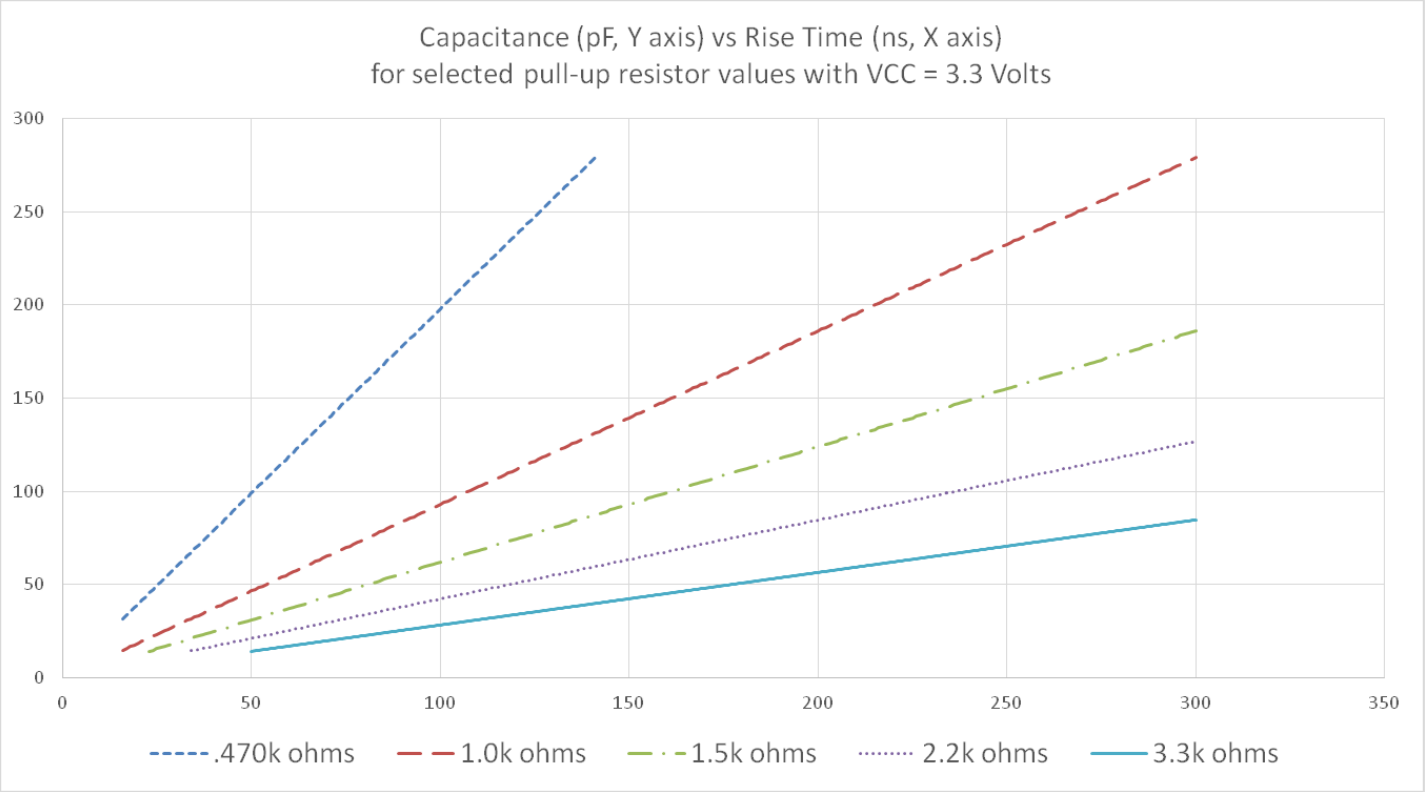


Figure 19: SDA/SCL options for pull-up resistor, bus capacitance and rise/fall times

5.6 Management Interface and Timing

A management memory interface (such as CMIS [5], SFP+ MIS [33]) and commonly used in other form factors like QSFP-DD, SFP-DD, or SFP+ enables module functionality and flexibility beyond that supported by the dedicated hardware signals. Read/Write functionality and protocols are defined in SFP-8419 [29].

Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page 00 is used to advertise SFP112 using CMIS memory map [5] vs SFP+/SFP28 using SFF-8472 memory map [33]. When a classic SFP+/SFP28 module is inserted into an SFP112 port the host must use the SFP+/SFP28 memory map (i.e., SFF-8472 [33]).

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

Timing requirements for the TWI signals, SCL and SDA are compatible with NXP I2C-bus specifications [19].

5.6.1 Management Timing Specification

The SFP112 TWI and memory management timing illustrated in in Figure 20 and the parameters given in Table 16. Implementations compliant to these specifications ensure compatibility between host bus initiator and the TWI.

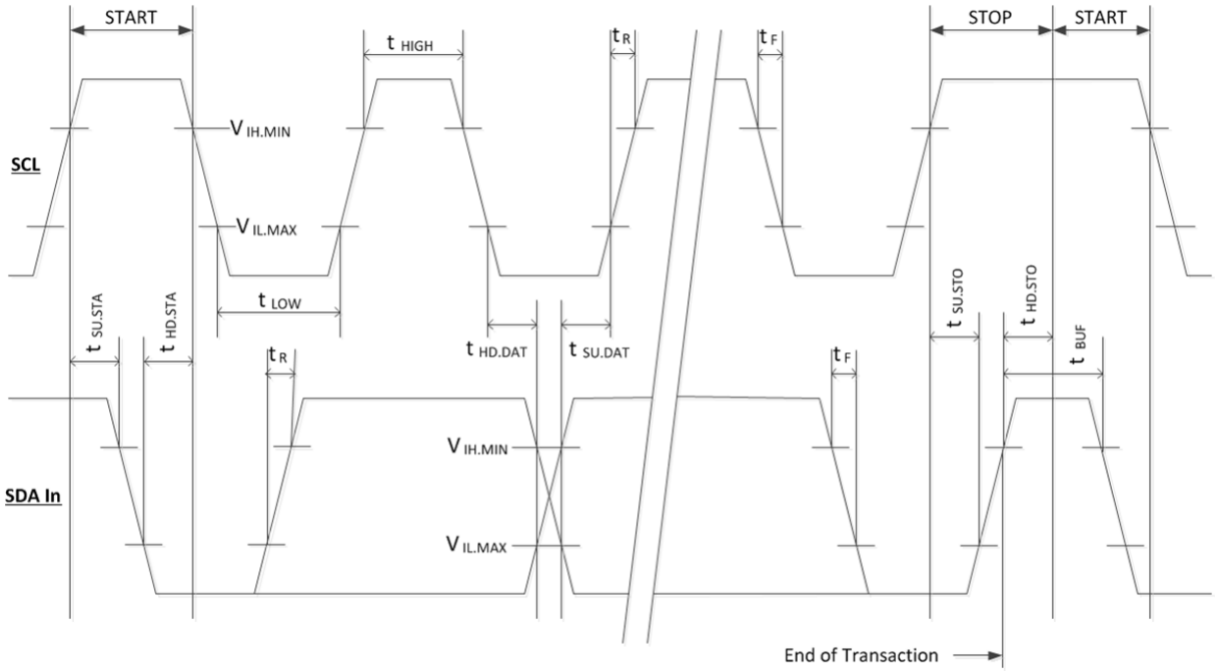


Figure 20: SFP112 Two Wire Interface Timing

Table 16- Management Interface timing parameters

Parameters	Symbol	Min	Max	Min	Max	Unit	Conditions
		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.50		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		20		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time	t_R		300		120	ns	From (VIL, MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	t_F		300		120	ns	From (VIH, MIN=0.7*Vcc) to (VIL, MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		0.26		µs	
STOP Hold Time	tHD.STO	0.6		0.26		µs	
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500		500	µs	Maximum time the SFP112 module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		80		80	ms	Complete (up to) 8 Byte Write
Accept a single or sequential write to volatile memory	tNACK		10		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50K		50k		cycles	Module Case Temperature = 70 ^oC

5.6.1.1 Bus timing tBUF

The timing attribute tBUF is the bus free time between sequential TWI transactions, see Figure 21. It’s measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

5.6.1.2 Bus timing tWR

The timing attribute tWR is the time required for a module to complete its internally timed write cycle after a single or sequential write to non-volatile memory before the next basic management operation can be accepted, see Figure 21. It’s measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

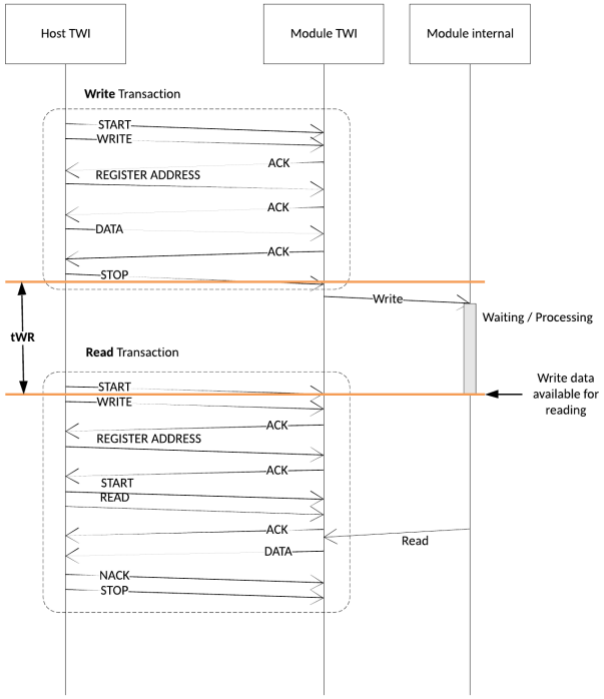


Figure 21: Bus timing tWR

5.6.1.3 Bus timing tNACK

The timing attribute tNACK is the time required for a module to complete its internally timed write cycle after a single or sequential write to volatile memory before the next basic management operation can be accepted, see Figure 22. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

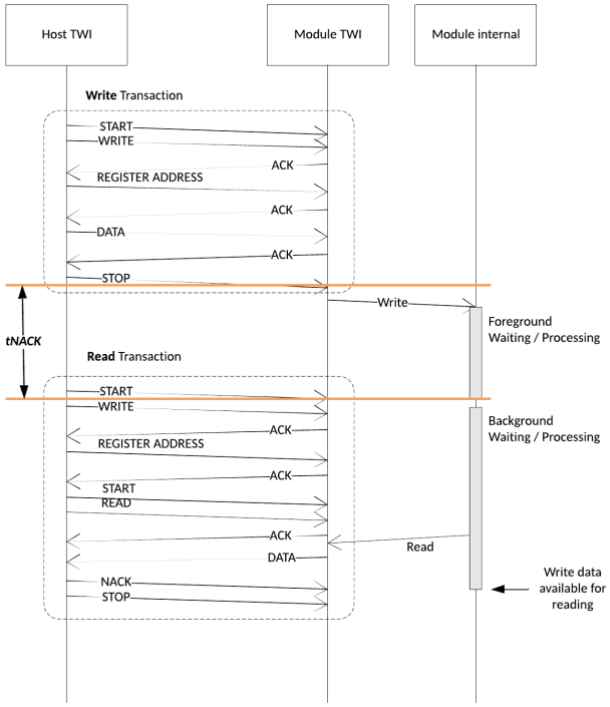


Figure 22: Bus timing tNACK

5.6.1.4 Bus timing tBPC

The timing attribute tBPC is the time required for a module to complete the change for the requested Bank and/or Page selection, see Figure 23. It's measured from the low to high SDA edge of the Stop condition of the Write transaction to the high to low SDA edge of the Start condition for the next transaction.

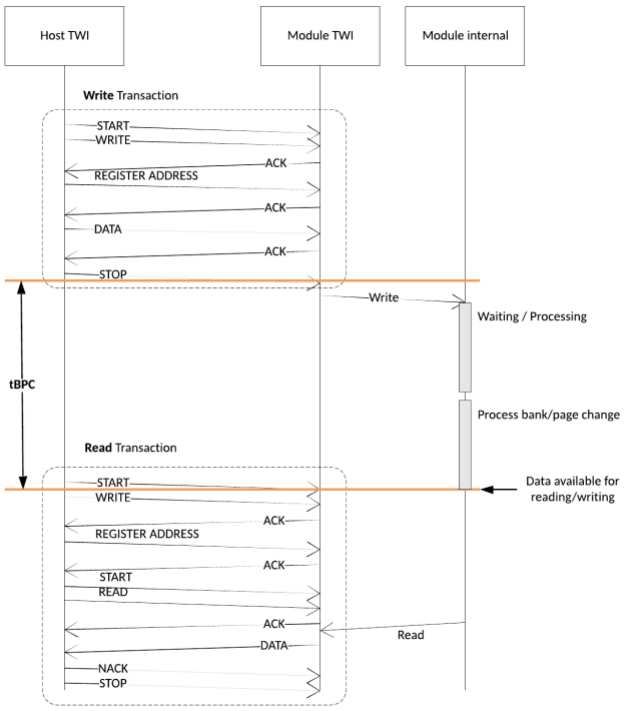


Figure 23: Bus timing tBPC

5.7 Timing for soft control and status functions

Timing for SFP112 soft control and status functions are described in Table 17. Squelch and disable timings are defined in Table 18.

Table 17- Timing for SFP112 soft control and status functions

Parameters	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1] to hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[2] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, TXFault and other flag bits.
Rx LOS Assert Time	ton_los		200	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b), LOS signal asserted and IntL asserted [4].
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and LOS signal asserted IntL asserted [4].
TXFault Assert Time	ton_TxFault		200	ms	Time from TXFault state to TXFault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[3] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[3] until associated IntL operation resumes
DataPathDeinit Max Duration[5]	DataPathDeinit_MaxDuration				see CMIS memory P01h: B144
DataPathInit Max Duration[5]	DataPathInit_MaxDuration				see CMIS memory P01h: B144
Module Pwr Up Max Duration[6]	ModulePwrUp_MaxDuration				see CMIS memory P01h: B167
ModulePwrDn Max Duration[6]	ModulePwrDn_MaxDuration				see CMIS memory P01h: B167
Data Path TX Turn On Max Duration[5]	DataPathTxTurnOn_MaxDuration				see CMIS memory P01h: B168
Data Path TX Turn Off Max Duration[5]	DataPathTxTurnOff_MaxDuration				see CMIS memory P01h: B168

Notes:
1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 21.
2. Measured from low to high SDA edge of the Stop condition of the read transaction.
3. Measured from low to high SDA edge of the Stop condition of the write transaction.
4. Rx LOS condition is defined at the optical input by the relevant standard.
5. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol, unless the module advertises a less than 1 ms duration in which case there is no defined measurement.
6. Measured from the low to high SDA edge of the Stop condition of the Write transaction until the IntL for the state change Vout:IntL=Vol.

Table 18- I/O Timing for Squelch & Disable

Parameters	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	100	ms	Time from loss of Rx input signal until the squelched output condition is reached, see 5.8.1
Rx Squelch Deassert Time	toff_Rxsq	10	s	Time from resumption of Rx input signals until normal Rx output condition is reached, see 5.8.1
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached, see 5.8.2
Tx Squelch Deassert Time	toff_Txsq	10	s	Time from resumption of Tx input signals until normal Tx output condition is reached, see 5.8.2
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence [1] until optical output falls below 10% of nominal, see note 2 and 3.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal, see note 2 and 3.
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 2 and 3.
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled

Notes:
1. Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.
2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.
3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

5.8 High Speed Electrical Specifications

For detailed electrical specifications see the appropriate specification, e.g. IEEE Std 802.3-2018 [12]; IEEE Std 802.3cd [13], 802.3ck [14]; FC-PI-6 [1], FC-PI-7[2], FC-PI-8 [3]; OIF-CEI-4.0 [20], or the InfiniBand specifications [16].

Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations given in clause 5.8.1 and 5.8.2 may be used.

5.8.1 RD0+, RD0-

RD(n)+/- are SFP112 module receiver data outputs. Rx(n)+/- are AC-coupled 100 Ω differential lines that should be terminated with 100 Ohms differentially at the Host ASIC(SerDes). The AC coupling is inside the SFP112 module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on optical lane/lanes becomes equal to or less than the level required to

assert LOS, then the electrical receiver output shall be squelched. SFP112 may have one or more Rx optical lanes associated with the electrical Rx output as shown in Table 24. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

5.8.2 TD0+, TD0-

TD(n)+/- are SFP112 module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the SFP112 optical module. The AC coupling is implemented inside the SFP112 optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter TX Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on electrical input channel is less than 70 mVpp, the transmitter optical output/outputs shall be squelched and the associated TxLOS flag set. The loss of the incoming electrical input channels causes the optical output channel/channels to be squelched.

For applications, e.g., Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where TX Squelch is implemented, the default case has TX Squelch active. TX Squelch can be deactivated using TX Squelch Disable through the 2-wire serial interface. TX Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

5.9 Rate Select Hardware Control

The module provides 2 inputs Speed1 and Speed2 that can optionally be used for rate selection as defined in Table 19. Speed1 controls the receive ^{path} signaling rate and Speed2 controls the transmit path signaling rate capability.

The rate select functionality can also be controlled by software as defined by the SFP112 management specification.

For 64 GFC FC-PI-8 [3] operation link speed is determined with FC Link Speed Negotiation (LSN) exchange while the link is operating at 32 GFC.

Table 19- Rate Select Hardware Control

Parameters	State	Conditions
Speed1	Low	RX signaling rate of 14.025 GBd (16 GFC)[1]
	High	RX signaling rate of 28.05 GBd (32 GFC)
Speed2	Low	TX signaling rate of 14.025 GBd (16 GFC) [1]
	High	TX signaling rate of 28.05 GBd (32 GFC)
Note 1: For SFP112 operating at 128 GFC there is no requirement for 16 GFC or rate select.		

5.10 Power Requirements

SFP112 has two designated power supply pins VccT and VccR in the connector. Power is applied concurrently to VccT and VccR.

A host board together with the SFP112 module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 21 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

5.10.1 Power Classes and Maximum Power Consumption

SFP112 power classes are defined in Table 20. Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host identify the power class of the module before allowing the module to go into high power mode.

Power levels associated with classifications of modules are shown in Table 20.

Table 20- Power Classification

Power Class	Max Power (W)	CMIS Register
1	1.0	Direct readout of Page 00h Byte 200[000xxxxx]
2	1.5	Direct readout of Page 00h Byte 200[001xxxxx]
3	2.0	Direct readout of Page 00h Byte 200[010xxxxx]
4	3.5	Direct readout of Page 00h Byte 200[011xxxxx]
5	5.0	Direct readout of Page 00h Byte 200[100xxxxx]
6	reserved	NA
7	reserved	NA
8[1]	> 5 W	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8 the host must read CMIS Page 00h Byte 201 to determine module power dissipation. Please see CMIS Byte 201 register definition for more information.		

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

5.10.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 24.

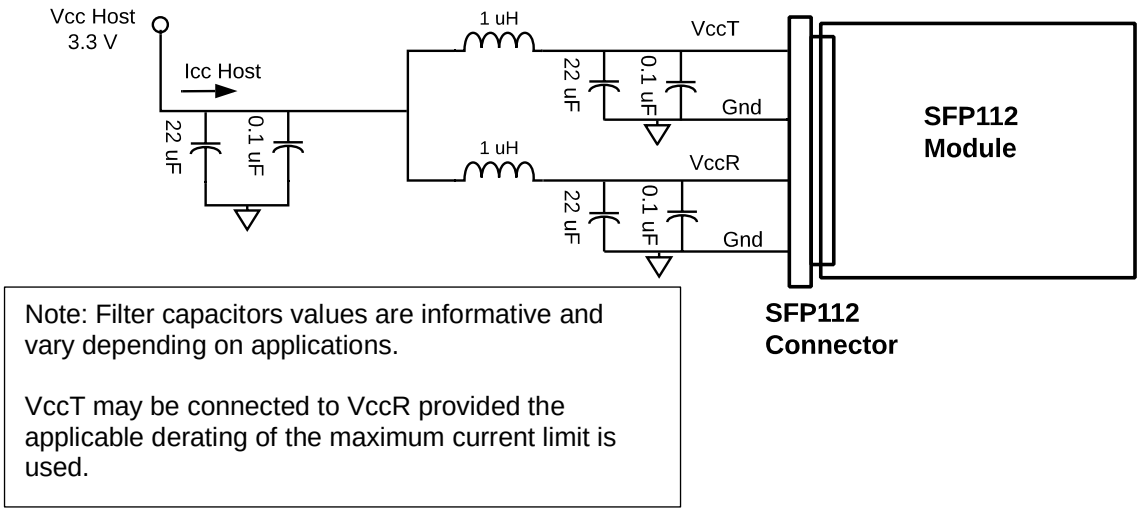


Figure 24: SFP112 Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 μF capacitors each have an equivalent series resistance of 0.22 ohms.

The specifications for the power supply are shown in Table 21. The limits in Table 21 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 24). An example test method for measuring inrush current can is Keysight Technologies application brief 5991-2778EN.pdf.

5.10.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all SFP112 modules shall power up in Low Power Mode if TxDisable is asserted. If TxDisable is not asserted the module will proceed to High Power Mode without host intervention. Figure 25 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 21.

Table 21- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1 including ripple, droop and noise below 100 kHz[1]		3.135	3.3	3.465	V
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Low Power Mode[2]					
Power Consumption	P_lp		.5		W
Instantaneous peak current at hot plug	Icc_ip_lp	-	200		mA
Sustained peak current at hot plug	Icc_sp_lp	-	165		mA
Steady state current	Icc_lp	See Note 4			mA
High Power Class 1 module					
Power Consumption	P_1		1.0		W
Instantaneous peak current	Icc_ip_1	-	400		mA
Sustained peak current	Icc_sp_1	-	330		mA
Steady state current	Icc_1	See Note 4			mA
High Power Class 2 module					
Power Consumption	P_2		1.5		W
Instantaneous peak current	Icc_ip_2	-	600		mA
Sustained peak current	Icc_sp_2	-	495		mA
Steady state current	Icc_2	See Note 4			mA
High Power Class 3 module					
Power Consumption	P_3		2.0		W
Instantaneous peak current	Icc_ip_3	-	800		mA
Sustained peak current	Icc_sp_3	-	660		mA
Steady state current	Icc_3	See Note 4			mA
High Power Class 4 module					
Power Consumption	P_4		3.5		W
Instantaneous peak current	Icc_ip_4	-	1400		mA
Sustained peak current	Icc_sp_4	-	1155		mA
Steady state current	Icc_4	See Note 4			mA
High Power Class 5 module					
Power Consumption	P_5		5.0		W
Instantaneous peak current	Icc_ip_5	-	2000		mA
Sustained peak current	Icc_sp_5	-	1650		mA
Steady state current	Icc_5	See Note 4			mA
High Power Class 8 module					
Power Consumption	P_8[3]				W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	4	A

Notes:
1. Measured at VccT, VccR, VccT1, and VccR1.
2. Host designers are responsible for handling 1.5W Low Power Mode SFP(INF-8074i)/SFP+(SFF-8431) classic modules as appropriate in their system.
3. User must read management register for maximum power consumption.
4. The module must stay within its declared power class.

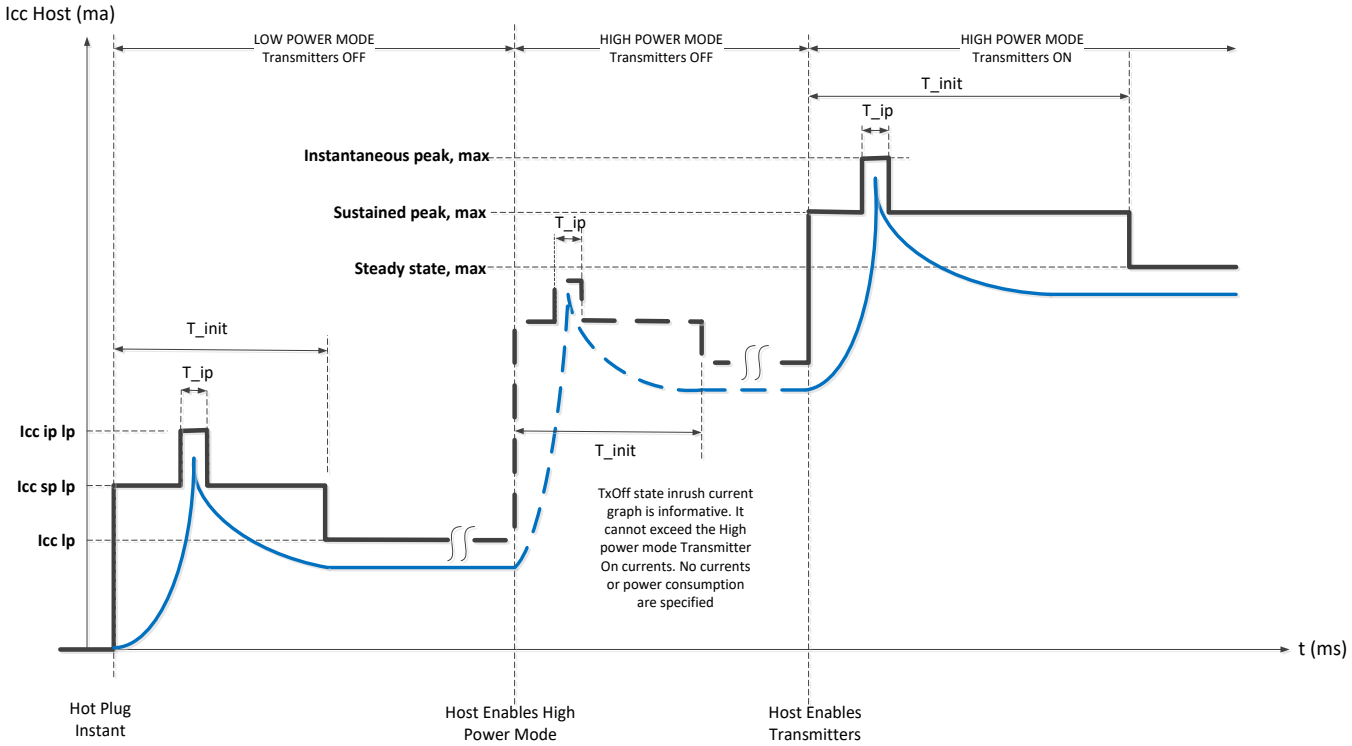


Figure 25: Instantaneous and sustained peak currents for Icc Host (see Table 21)

5.10.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the eN_Host value in Table 21 when tested by the methods of SFF-8431 [30] D.17.1 with the following exceptions:

a. The truncated function equation with coefficients from Table 22.
b. The resistor shall draw the maximum rated current per contact.
c. The frequency response of the truncated function is illustrated in Figure 26.

Table 22- Truncated Filter Response Coefficients for Host Power Supply Noise Output

Frequency	a	b	c	d	e
10 Hz ≤ f ≤ 240.2 Hz	0	0	0	0	-0.1
240.2 Hz ≤ f ≤ 24.03 kHz	0.3784	-3.6045	12.694	-19.556	11.002
24.03 kHz ≤ f ≤ 360.4 kHz	-22.67038	430.392	-3053.779	9574.26	-11175.98
360.4 kHz ≤ f ≤ 12.6 MHz	3.692166	-91.467	838.80	-3400.38	5139.285
12.6 MHz ≤ f ≤ 24 MHz	0	0	0	0	-60

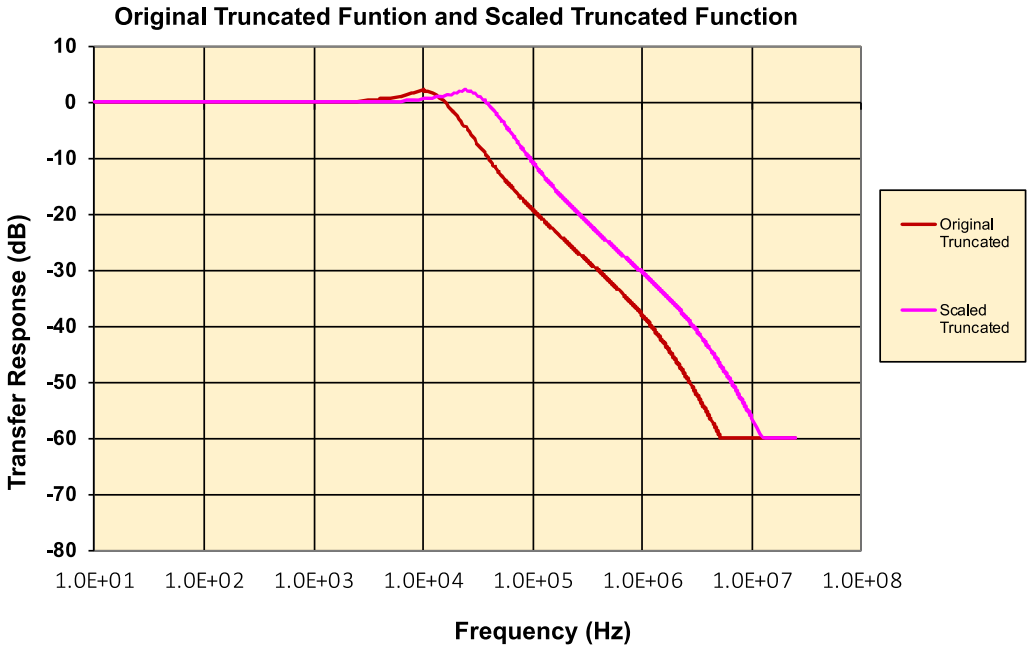


Figure 26: Truncated Transfer Response for Host Board Power Supply Noise Output measurement

5.10.5 Module Power Supply Noise Output

The SFP112 modules when plugged into a reference module compliance board shall generate noise less than the value in Table 21 when tested by the methods of SFF-8431[30], D.17.2. The module must pass module power supply noise output test in all operating modes. This test ensures the module will not couple excessive noise from inside the module back onto the host board.

The RMS module noise voltage output is defined in the frequency band from 10 Hz to 10 MHz. Module noise shall be measured with an appropriate probing technique at the input stage of the Vcc PSU filtering network, see Figure 27.

5.10.6 Module Power Supply Noise Tolerance

The SFP112 modules shall meet all requirements and remain fully operational in the presence of a reference noise waveform described in Table 23 superimposed on the DC voltage. The reference noise waveform consists of triangular sweep of supply voltage Vcc PSU from 3.135 to 3.465 while a sinusoidal 1 kHz to 1 MHz noise is added to Vcc PSU. This emulates the worst case noise the module must tolerate and be fully operational. The reference noise shall be injected at the input stage of the Vcc PSU filtering network, see Figure 27. An appropriate probing technique is required for noise characterization.

Table 23- Power Supply Output Noise and Tolerance Specifications

Parameter	Symbol	Min	Nom	Max	Unit
Host RMS noise output 40 Hz-10 MHz (eN_Host)				25	mV
Module RMS noise output 10 Hz - 10 MHz				30	mV
Module sinusoidal power supply noise tolerance 1 kHz - 1 MHz (p-p) [1]	$PSNR_{mod}$			66	mV
Vcc PSU triangular tolerance waveform amplitude (p-p) [2]		3.135		3.465	V
Vcc PSU triangular tolerance waveform frequency (p-p)		0.001		1000	Hz
Notes: 1. Module sinusoidal power supply noise must be added to the Vcc PSU triangular waveform. 2. Assumes nominal Vcc PSU=3.3 V.					

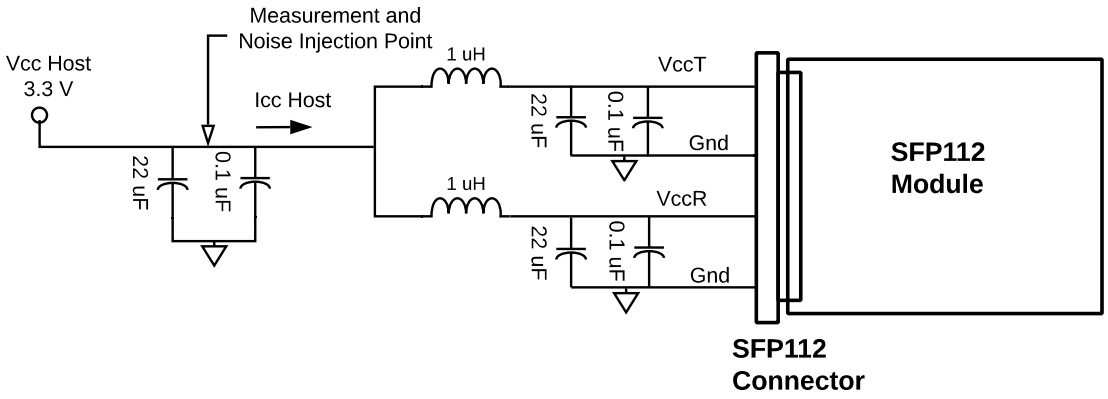


Figure 27: Module Noise Injection Point

5.11 ESD

Where ESD performance is not otherwise specified, e.g., in the InfiniBand specification, the SFP112 module shall meet ESD requirements given in EN61000-4-2 [8], criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15 kV air discharges during operation and 8 kV direct contact discharges to the case. All the SFP112 module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001 [9].

6. Optical Port Mapping and Optical Interfaces

6.1 Electrical data input/output to optical port mapping

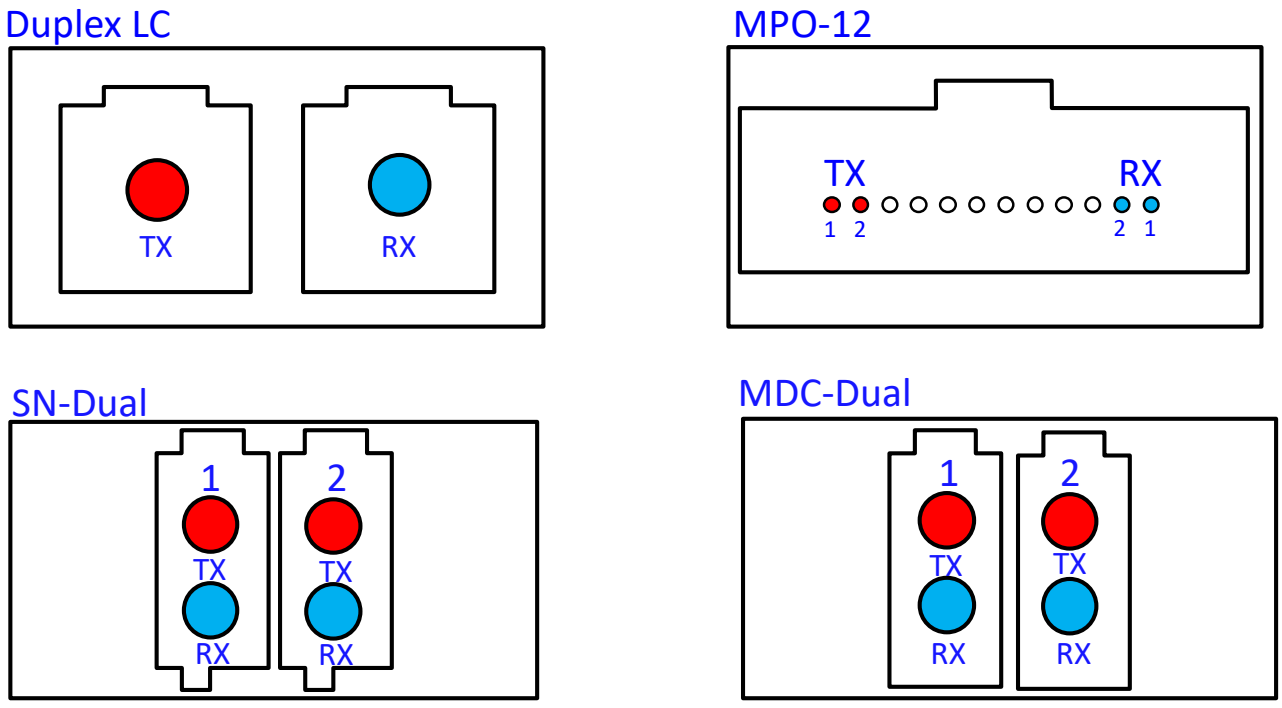
Table 24 defines the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Table 24- Electrical data input to Optical Port Mapping

Electrical Data Input Reference	LC, SN, MDC	SN, MDC, MPO-12
	1 TX fiber	2 TX fibers
TD0+/-	TX-1	TX-1
TD1+/-		TX-2

6.2 Optical Interfaces

Four examples of the SFP-DD/SFP-DD112 optical interface port are a male MPO receptacle (see Figure 24), a dual LC (see Figure 30), a SN receptacle (see Figure 33), or a MDC receptacle (see Figure 34). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 28.



Note: The transmit and receive optical lanes shall occupy the positions depicted here when looking into the MDI receptacle with the connector keyway feature on top.

Figure 28: Optical Media Dependent Interface port assignments

6.2.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5 [10], IEC 61754-7 [23] and shown in Figure 29. Note: Two alignment pins are present in each receptacle.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

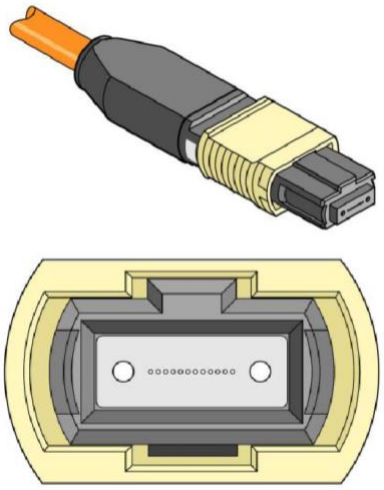


Figure 29: MPO-12 Single Row optical patch cord and module receptacle

6.2.2 Duplex LC Optical Cable connection

The Duplex LC optical patchcord and module receptacle is specified in TIA-604-10 [11], IEC 61754-20 [24] and shown in Figure 30.

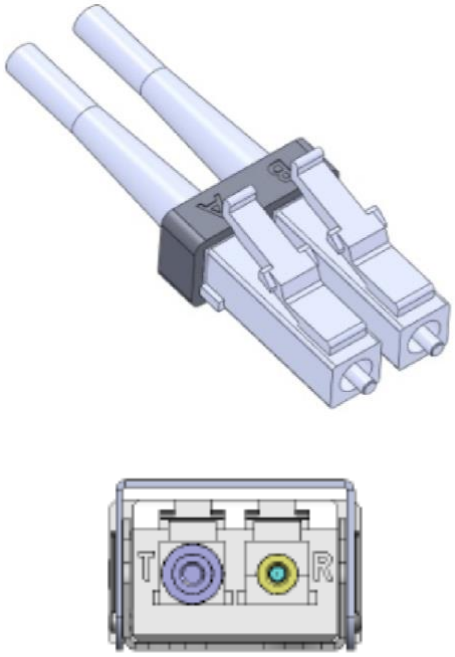


Figure 30: Duplex LC optical patchcord and module receptacle

LC connector latch extends up to 2.15 mm above the SFP-DD/SFP-DD112/SFP112 as shown in Figure 31. To avoid interference in stacked SFP-DD/SFP-DD112/SFP112 cages configurations the minimum vertical port pitch is 14.9 mm, see Figure 32.

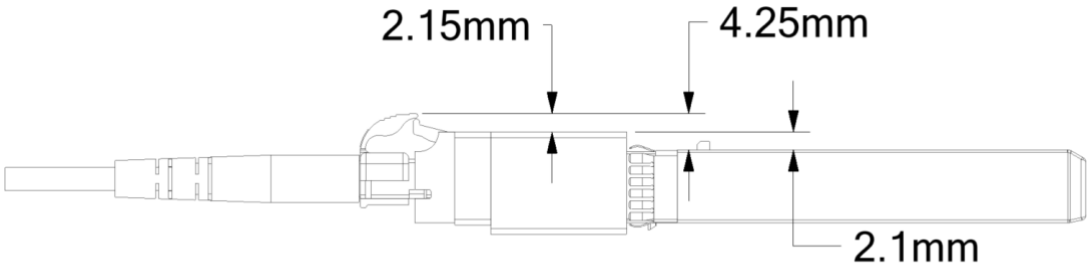


Figure 31: LC connector excursion above module nose height

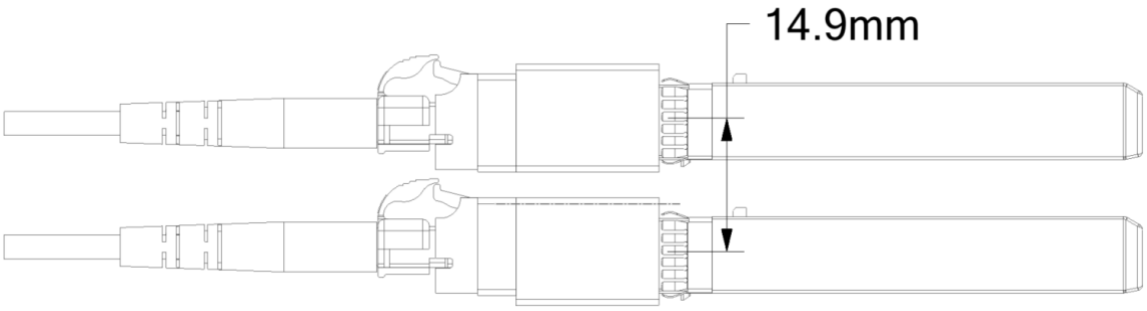


Figure 32: Minimum vertical port pitch

6.2.3 SN Optical Cable connections

The SN optical connector and receptacle for SFP-DD/SFP-DD112 module is specified in SN-60092019 [22] and shown in Figure 26. The top key and offset bottom key are used to ensure alignment between the modules and the patch cords.

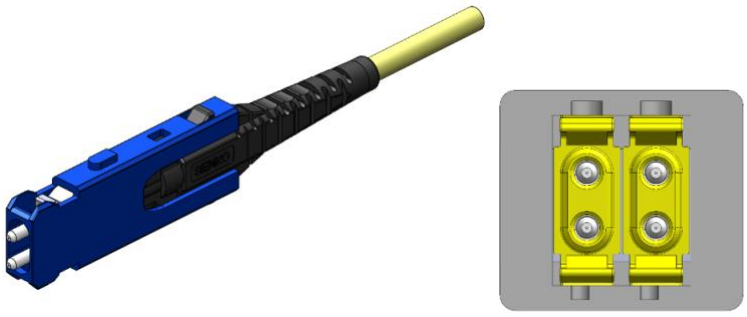


Figure 33: SN optical connector plug and two-port module receptacle

6.2.4 MDC Optical Cable connections

The MDC optical plug and receptacle for an SFP-DD/SFP-DD112 module is specified in USC-11383001 [25] and shown in Figure 27. The optical connector is orientated such that the keying feature of the MDC receptacle is on the top.

Figure 34: MDC optical connector plug and two-port module receptacle

6.3 Module Color Coding and Labeling

If provided, color coding shall be on an exposed feature of the SFP-DD/SFP-DD112 module (a feature or surface extending outside of the bezel). Color code are outside the scope of this specification.

Each SFP-DD/SFP-DD112 module shall be clearly labeled. The complete labeling need not be visible when the SFP-DD/SFP-DD112 module is installed, and the bottom of the device is the recommended location for the label. Labeling shall include:

- Appropriate manufacturing and part number identification
- Appropriate regulatory compliance labeling
- A manufacturing traceability code.

The label should also include clear specification of the external port characteristics such as:

- Optical wavelength
- Required fiber characteristics
- Operating data rate
- Interface standards supported
- Link length supported.

The labeling shall not interfere with the mechanical, thermal or EMI features.

7. SFP-DD Mechanical and Board Definition

7.1 Introduction to SFP-DD and SFP-DD112

The cages and modules specifications defined in this chapter are illustrated in Figure 35 (press fit cage) and Figure 36 (pluggable module). All Pluggable modules and direct attach cable plugs must mate to the connectors and cages defined in this specification. (See SFF-8432 [31]) Heat sink/clip thermal designs are application specific and not specifically defined by this specification. The SFP-DD and SFP-DD112 modules and cage support both a pull tab and a bail latch solution. Details on bail latch retention and extraction specifications can be found in SFF-8432.

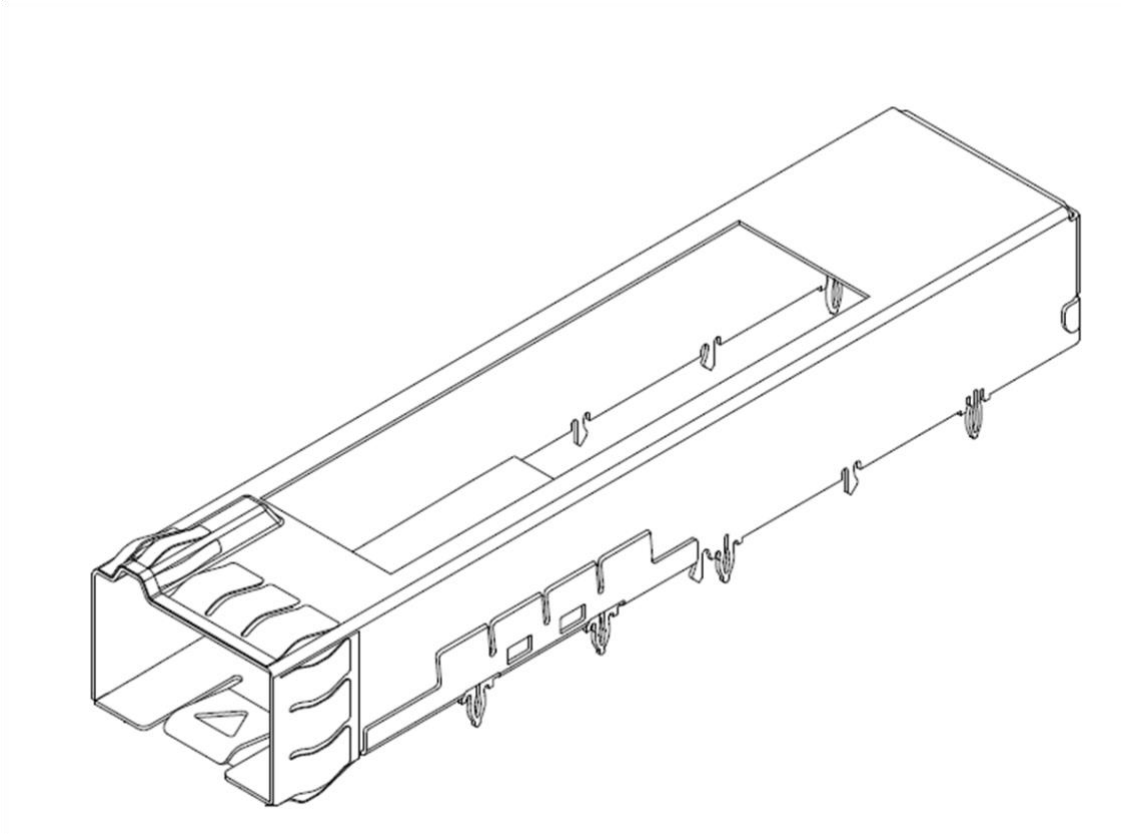
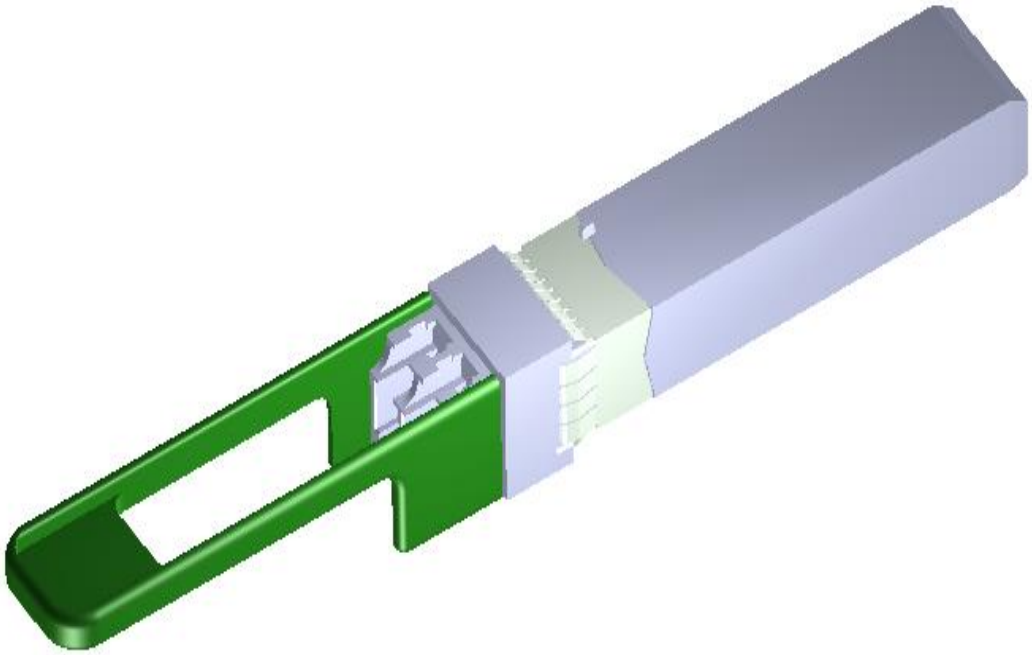
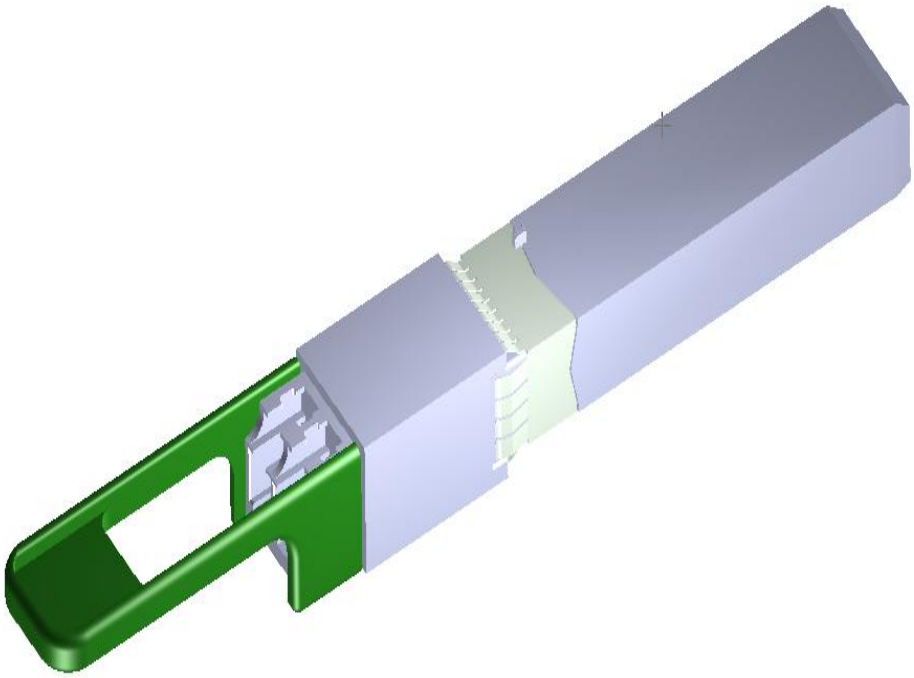


Figure 35: Press fit cage



Type 1 module



Type 2 module

Figure 36: SFP-DD and SFP-DD112 Modules

7.2 SFP-DD/SFP-DD112/SFP112 Datums, Dimensions and Component Alignment

A listing of the SFP-DD/SFP-DD112/SFP112 datums for the various components are contained in Table 25. To reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009 [4]. All dimensions are in millimeters.

Table 25- Datum Description

Datum	Description
A	Width Of module
B	Bottom surface of module
C	Leading edge of signal contact pads on module paddle card
D	Hard stop on module
E	Host board thru hole to accept primary cage press fit pin
F	Hard stop on cage
G	Bottom surface of bezel cutout
K	Host board thru hole #1 to accept connector guidepost
L	Host board thru hole #2 to accept connector guidepost
P	Vertical center line of internal surface of cage
S	Seating plane of cage on host board
Z	Top surface of host board
AA	Center line of module paddle card width
BB	Top surface of module paddle card
CC	Center line of connector slot width
DD	Seating plane of connector on host board

7.3 SFP-DD Cage, Connector, Module Alignment

The alignment of the cage, connector and module are shown in Figure 37.

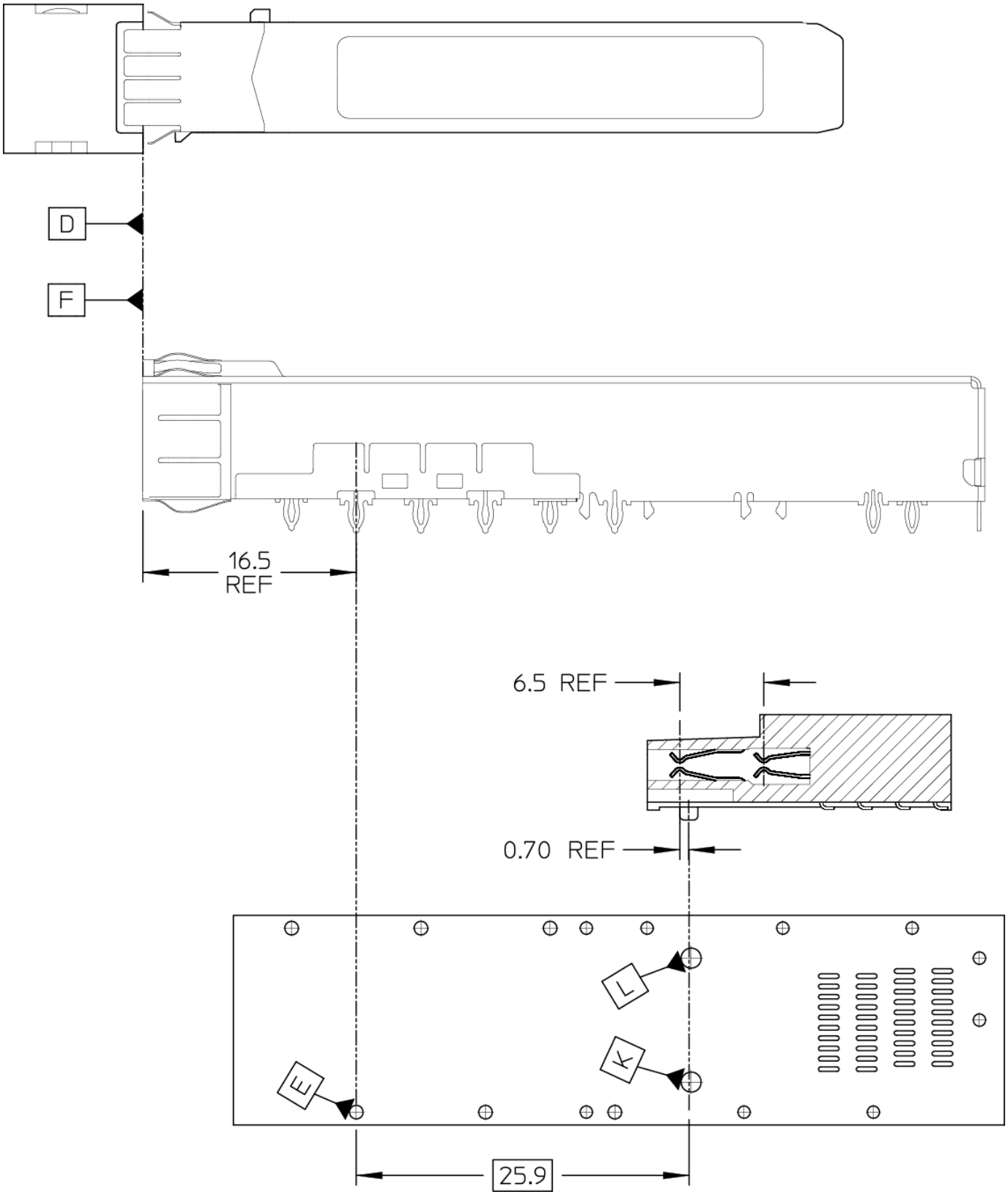
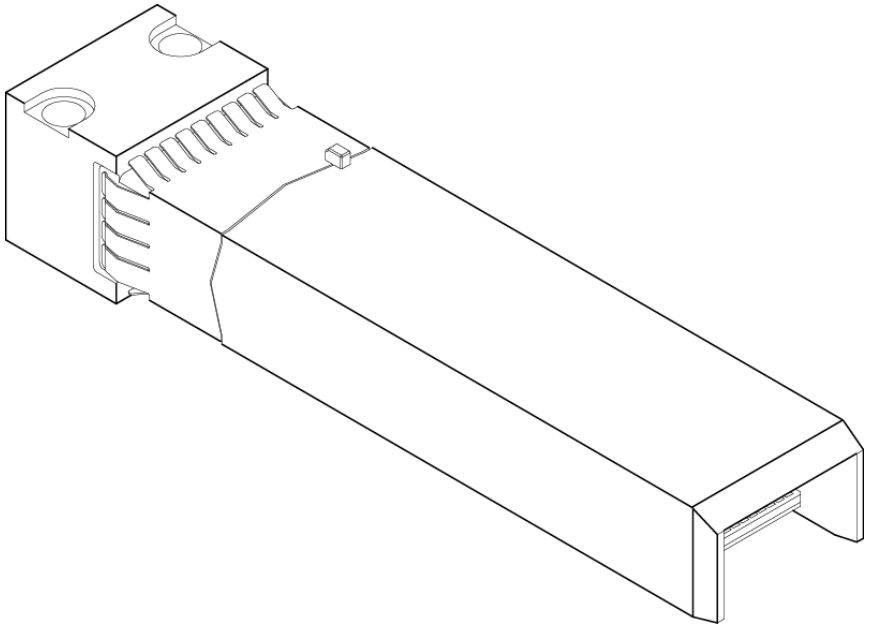


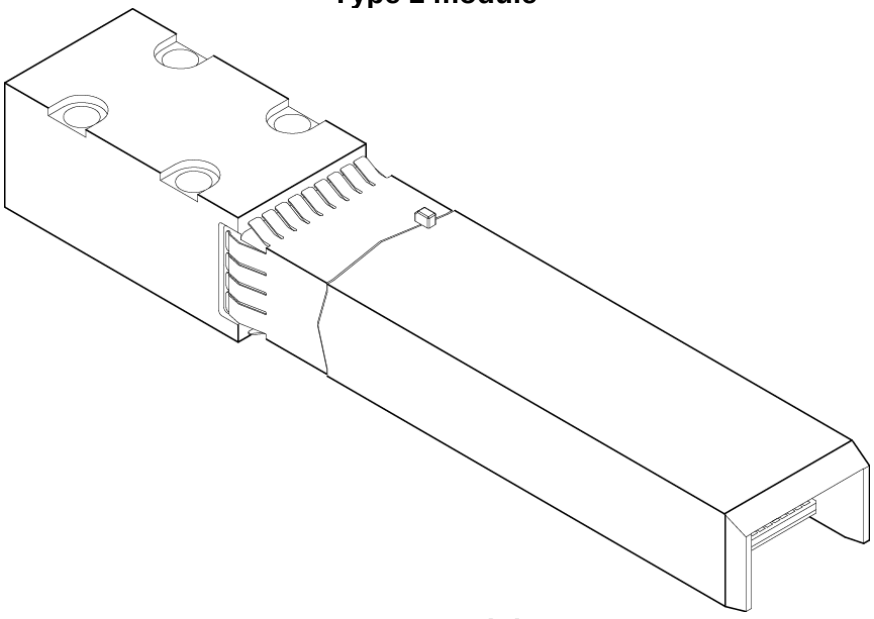
Figure 37: Cage, Connector alignment

7.4 SFP-DD/SFP-DD112 Module Mechanical Dimensions

The mechanical outline for the SFP-DD/SFP-DD112 modules and direct attach cables are shown in Figure 38. The module shall provide a means to self-lock with the cage upon insertion. The module package dimensions are defined in Figure 39. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 39.



Type 1 module



Type 2 module

Figure 38: Type 1 and Type 2 Modules

NOTES APPLY TO MODULE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS.

3 RECOMMENDED MAXIMUM. MODULE LENGTH EXTENDING OUTSIDE OF CAGE. OTHER LENGTHS ARE APPLICATION SPECIFIC.

4 INDICATED OUTLINE DEFINES MAXIMUM ENVELOP OUTSIDE THE CAGE. THE SURFACES OF THE MAXIMUM ENVELOP MAY BE CONTACTED BY AN ADJACENT MODULE EMI SPRINGS DURING INSERTION AND EXTRACTION OF THE MODULE FROM THE CAGE. THE SURFACES SHALL NOT HAVE ANY SHAPES OR MATERIALS THAT CAN DAMAGE THE ADJACENT MODULE EMI SPRINGS OR BE DAMAGED THEMSELVES BY THE SPRINGS.

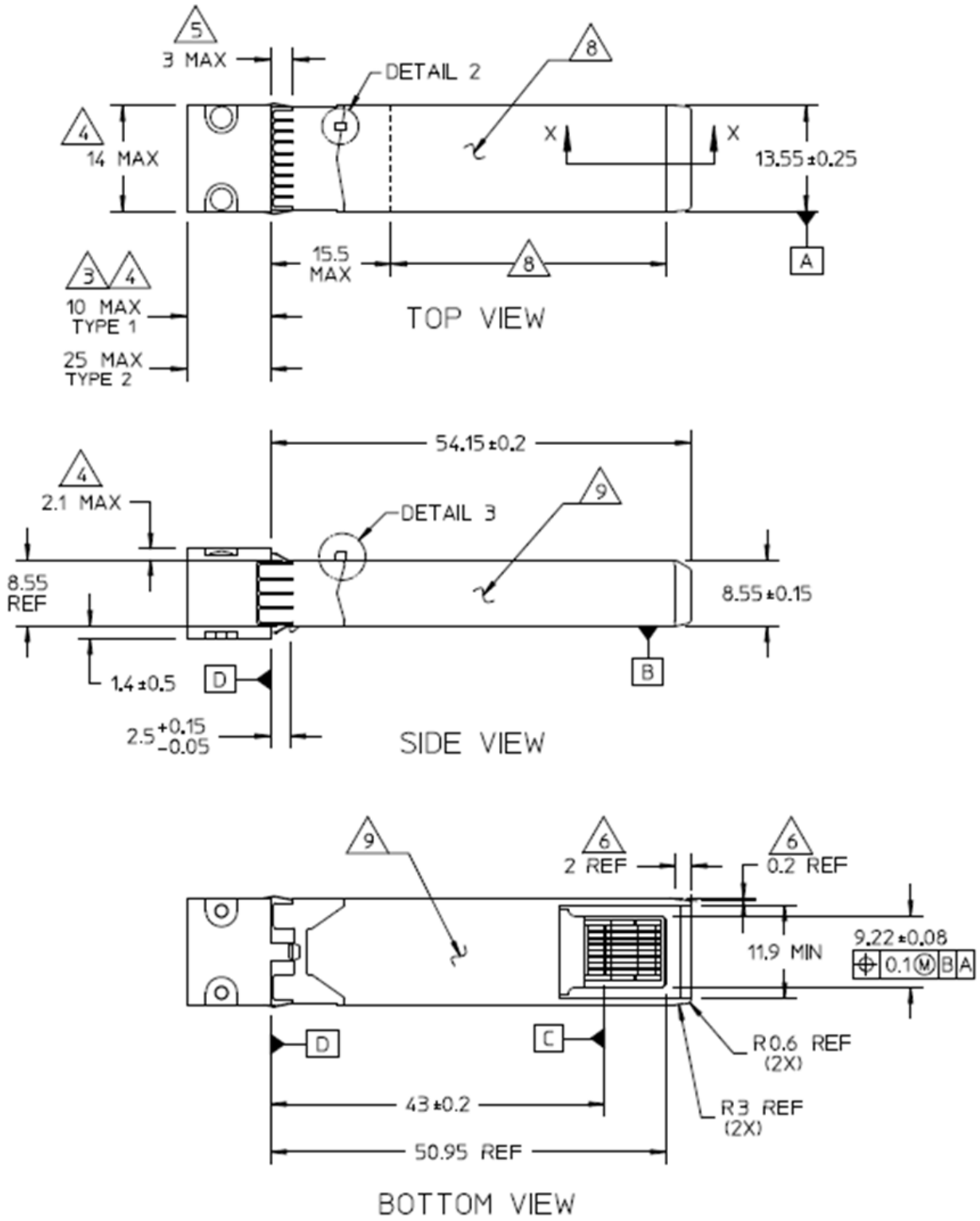
5 DIMENSIONS DEFINES EMI SPRING CONTACT POINT WITH MODULE CAGE.

6 LEAD-IN CHAMFER DIMENSION MEASURED FROM TSC (THEORETICAL SHARP CORNER).

7 BLOCKING RIB FEATURE TO PREVENT SFP-DD MODULE FROM MATING INTO LEGACY SFP CONNECTOR.

8 FLATNESS SPECIFICATION APPLIES OVER THE ENTIRE HEAT SINK AREA. REFER TO SECTION 5.4 TABLE 9FOR FLATNESS REQUIREMENTS.

9 PRODUCT LABEL ON BOTTOM AND/OR SIDES TO BE FLUSHED OR RECESSED BELOW EXTERNAL SURFACES. LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMC PROPERTIES.


5
3 MAX
DETAIL 2
8
4
14 MAX
X
X
13.55±0.25
A
3
4
10 MAX
TYPE 1
25 MAX
TYPE 2
15.5
MAX
8
TOP VIEW
54.15±0.2
4
2.1 MAX
DETAIL 3
9
8.55
REF
8.55±0.15
1.4±0.5
D
B
2.5 +0.15 −0.05
SIDE VIEW
9
6
2 REF
6
0.2 REF
11.9 MIN
9.22±0.08
0.1 M B A
D
C
R0.6 REF
(2X)
43±0.2
R3 REF
(2X)
50.95 REF
BOTTOM VIEW

1
2
3

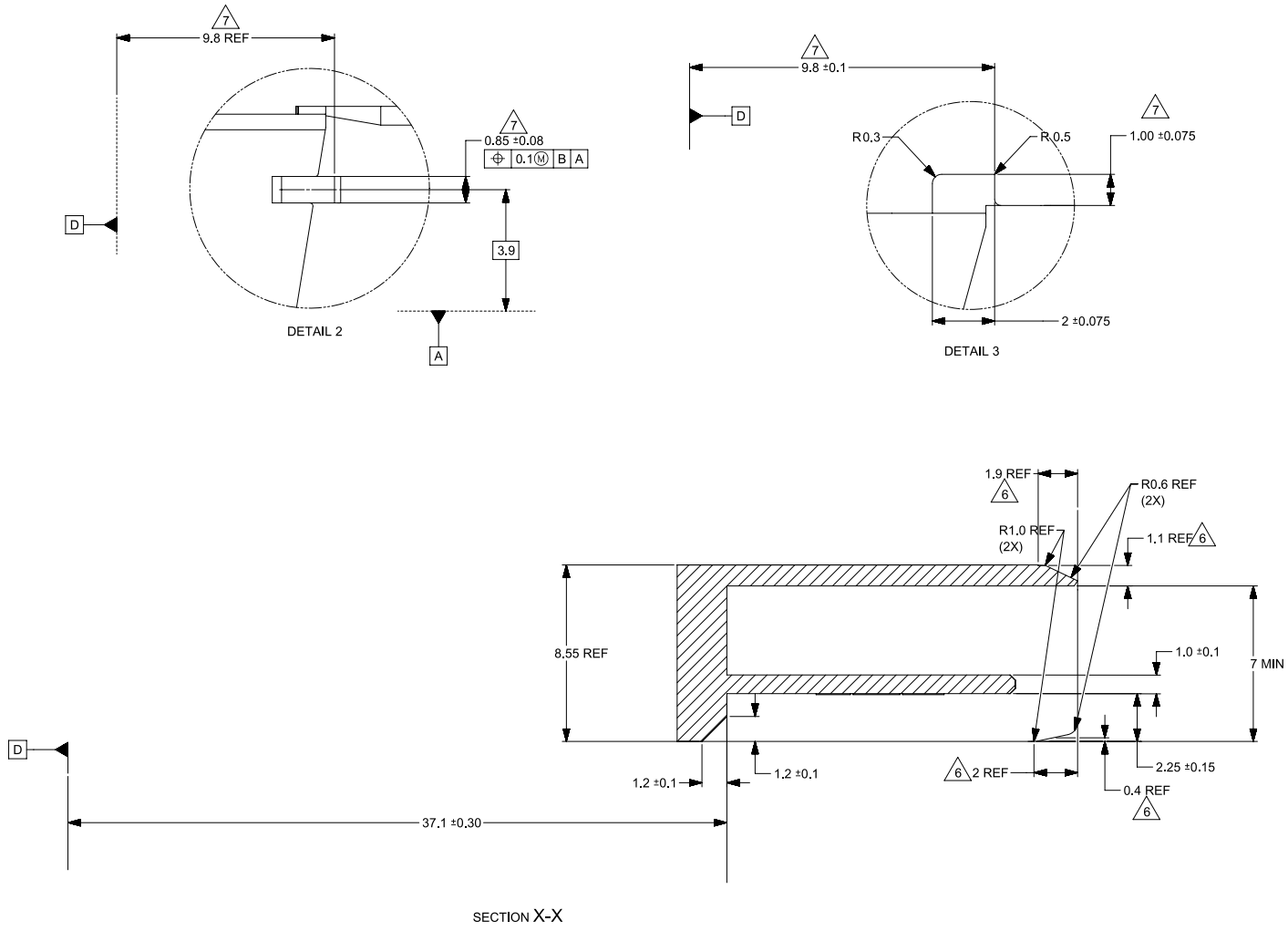


Figure 39: Detailed dimensions of module

7.5 SFP-DD/SFP-DD112/SFP112 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 39. Specifications for Module flatness and surface roughness are shown in Table 26.

Table 26- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	reserved	reserved
7	reserved	reserved
8	0.050	0.8

7.6 SFP-DD Module paddle card dimensions

NOTES APPLY TO MODULE PADDLE CARD :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD
5. DATUM C IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTER MOST SIGNAL CONTACTS PADS TO BE RE-ESTABLISHED ON EACH SIDE
6. DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS
7. DIMENSION AND TOLERANCE APPLIES TO ALL PADS ON BOTH TOP AND BOTTOM SIDE OF THE PADDLE CARD
8. A ZERO GAP IS ALLOWED FOR A CONTINUOUS PAD OPTION
9. APPLIES TO ALL SIGNAL PAD TO PRE-WIPE PAD SPACING
10. PRE-WIPE PADS (SHADED AREA) ON MODULE CARD HOST SIDE ARE OPTIONAL
11. PRE-WIPE PADS (UNSHADED AREA) ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND PAD DESIGNS
12. PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE
13. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS
14. MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS
15. COMPONENT KEEP OUT AREA MEASURED FROM DATUM C
16. A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED, THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OF 0.13 ± 0.05
17. PRE-WIPE PADS ENSURE ADEQUATE WIPE REQUIRED TO PROVIDE A RELIABLE ELECTRICAL INTERCONNECT WHILE MINIMIZING SIGNAL INTEGRITY STUB EFFECTS
18. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1.27 MICROMETERS MINIMUM NICKEL

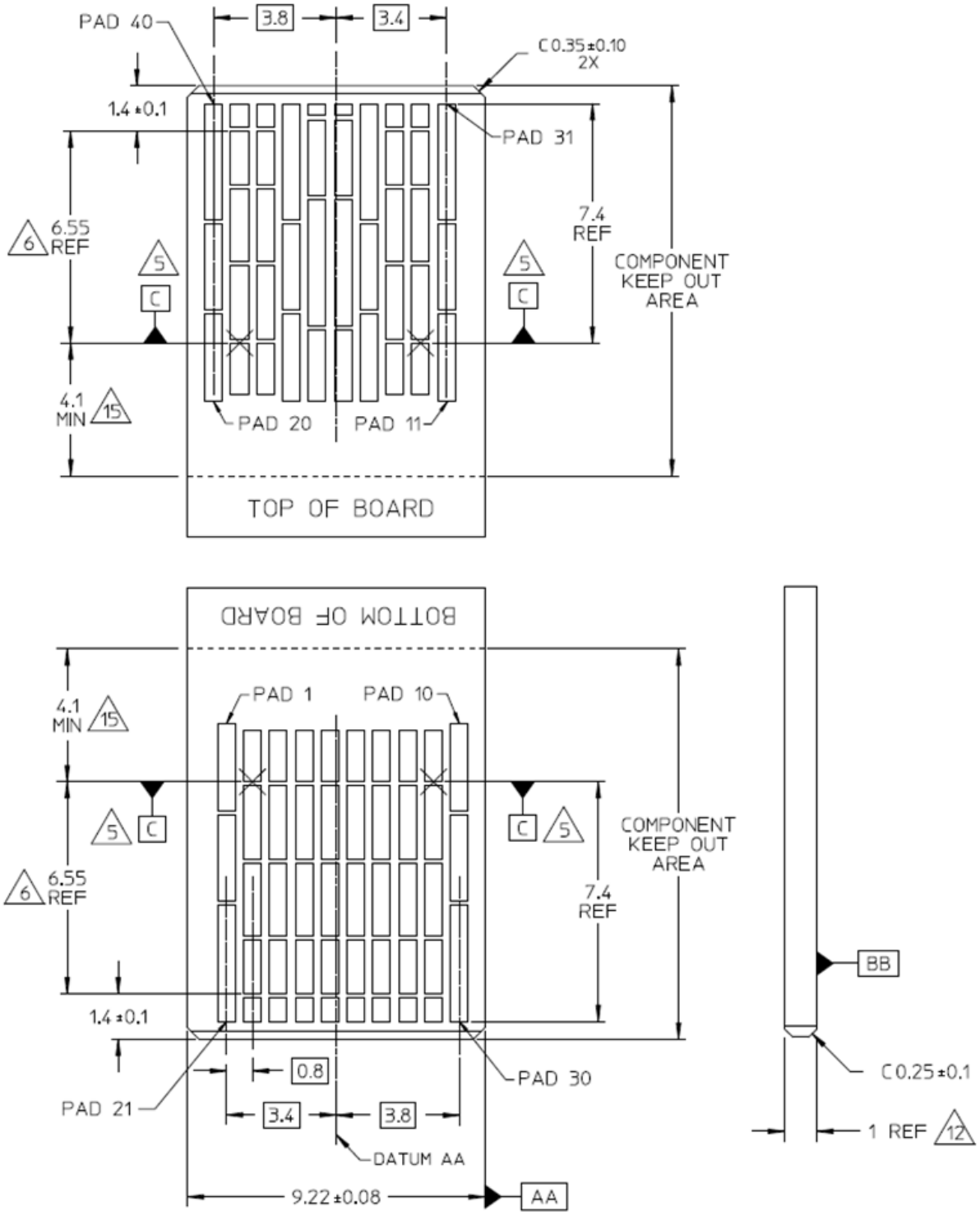


Figure 40: Module paddle card dimensions

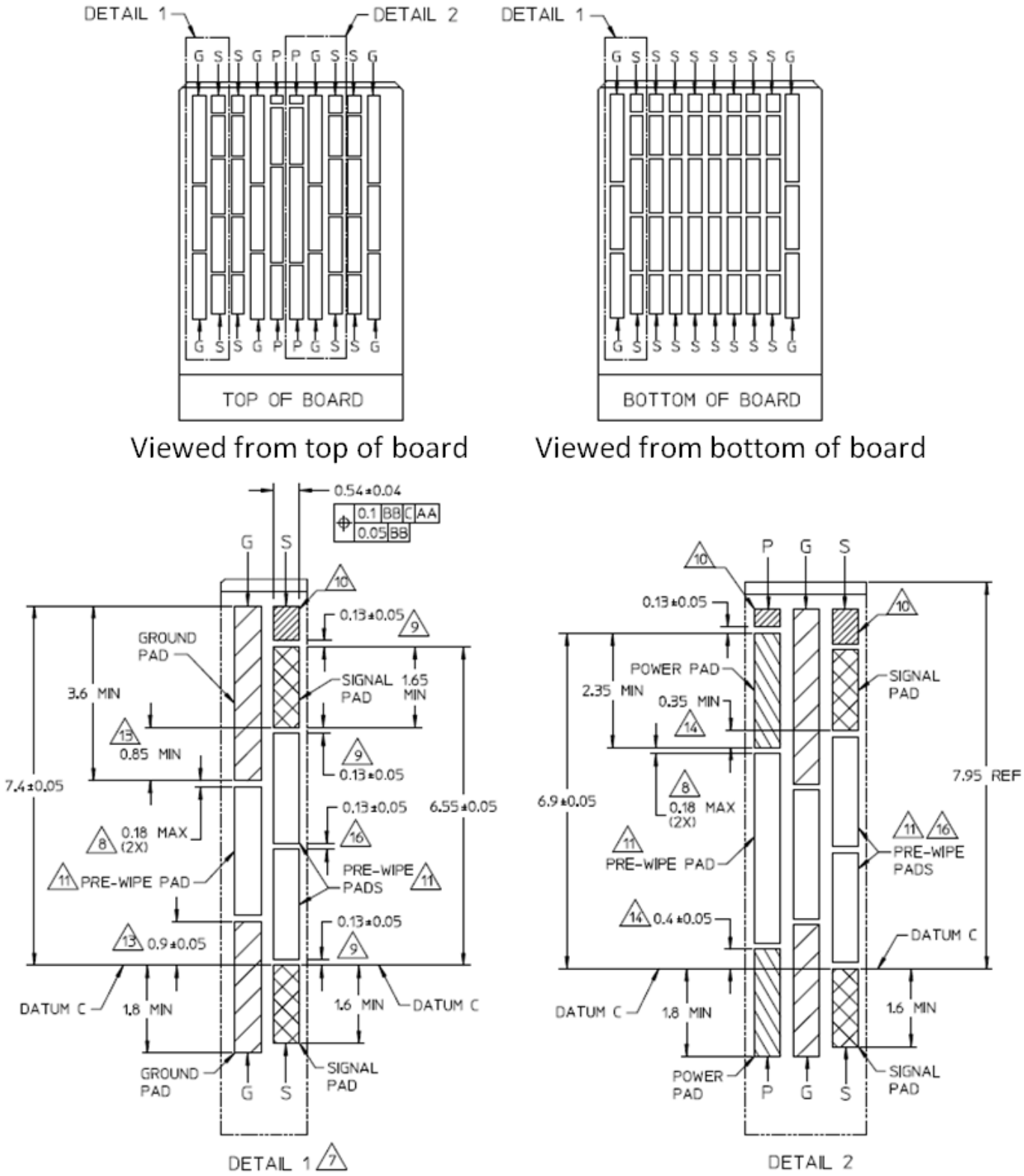


Figure 41: Module pad dimensions

7.7 SFP-DD/SFP-DD112/SFP112 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified Appendix A. The SFP-DD/SFP-DD112/SFP112 cage and modules are designed to ensure that excessive force applied to a cable does not damage the SFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. Examples of module retention mechanisms are found in SFF-8432 [31] Figures 4-4 through 4-7. The contact pad plating shall meet the requirements are given in 7.6.

7.8 Press fit Cage Mechanical

The SFP-DD Cage is shown in Figure 42 with detailed drawings in Figure 43. Recommendations for the cage bezel opening are shown in Figure 45.

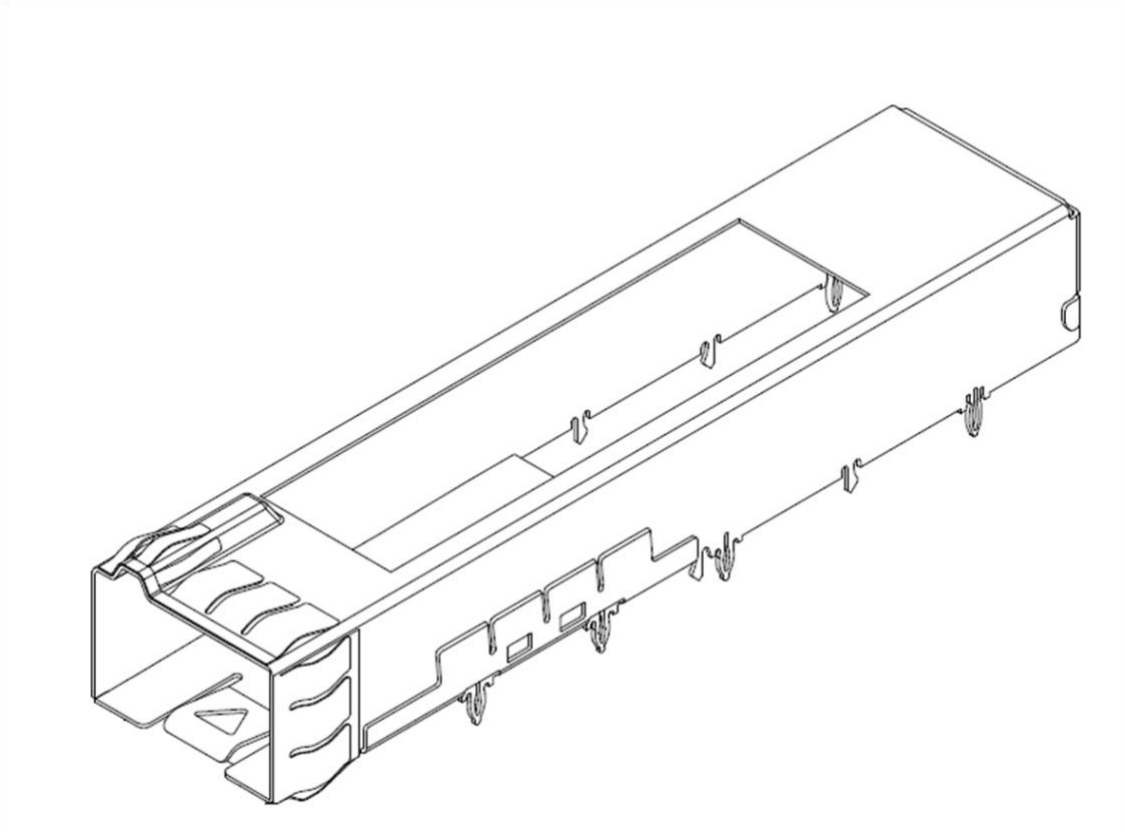


Figure 42: Press Fit 1x1 Cage

NOTES APPLY TO 1 X N CAGE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. DATUM S IS DEFINED BY THE SEATING SURFACE ON THE HOST BOARD

3. DIMENSIONS FROM INSIDE SURFACES OF CAGE

4. SIZE AND SHAPE OF CAGE PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

5. APPLIES TO 1.05 MM PCB HOLE DIAMETER

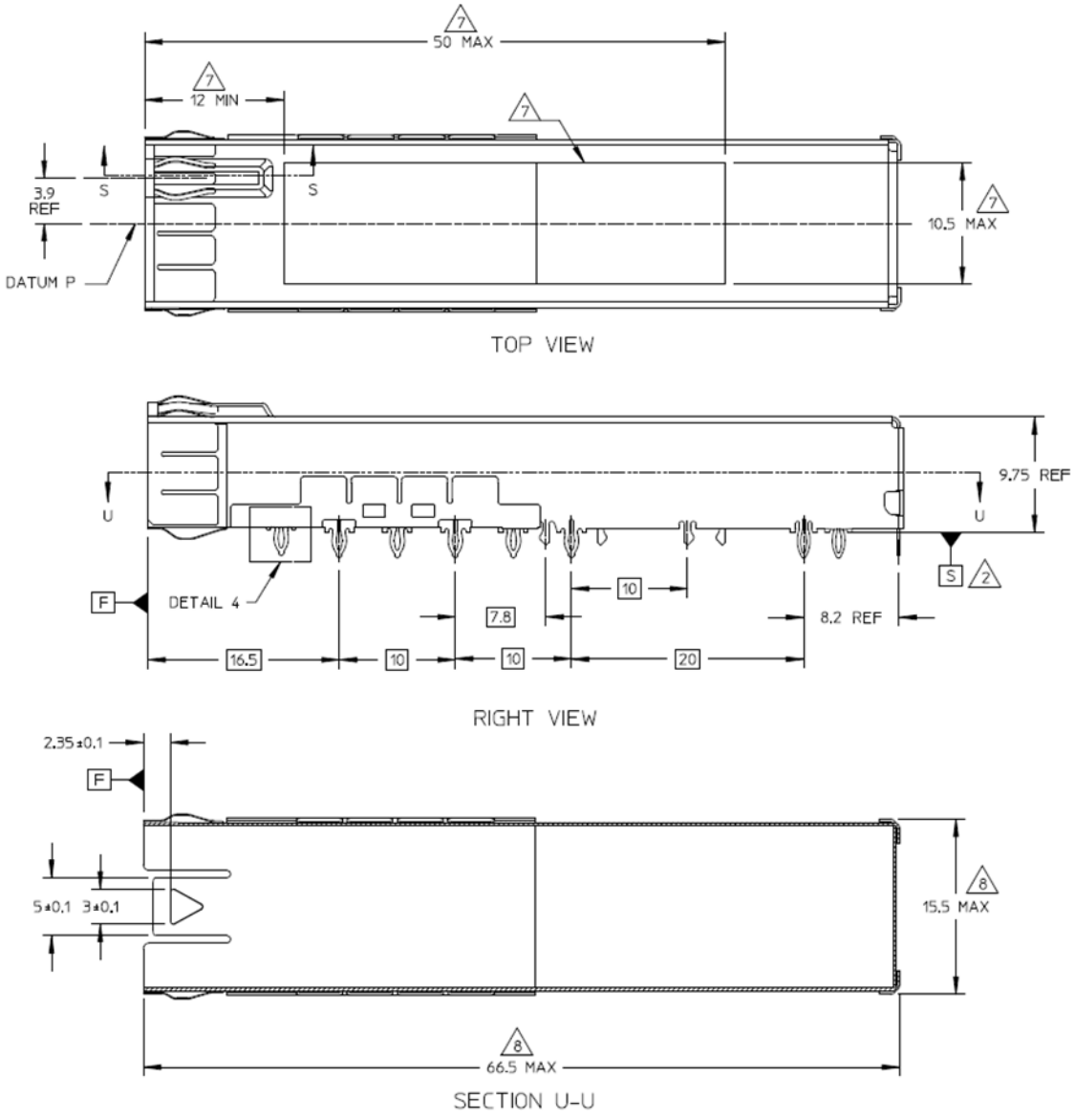
6. APPLIES TO 0.95 MM PCB HOLE DIAMETER

7. CUTOUT OPENING FOR HEAT SINK IS OPTIONAL

8. MAXIMUM ENVELOPE DIMENSION INCLUDES BACK COVER FOLDING TABS AND BOTTOM COVER ATTACHMENT FEATURES

9. APPLIES TO ALL RADAII SURFACES BETWEEN POINTS A AND B

10. APPLIES TO ALL FLAT SURFACES BETWEEN POINTS A AND B


7
50 MAX
7
12 MIN
7
3.9
REF
S
S
7
10.5 MAX
DATUM P
TOP VIEW
9.75 REF
U
U
S
2
F
DETAIL 4
10
7.8
8.2 REF
16.5
10
10
20
RIGHT VIEW
2.35±0.1
F
5±0.1
3±0.1
8
15.5 MAX
8
66.5 MAX
SECTION U-U

1

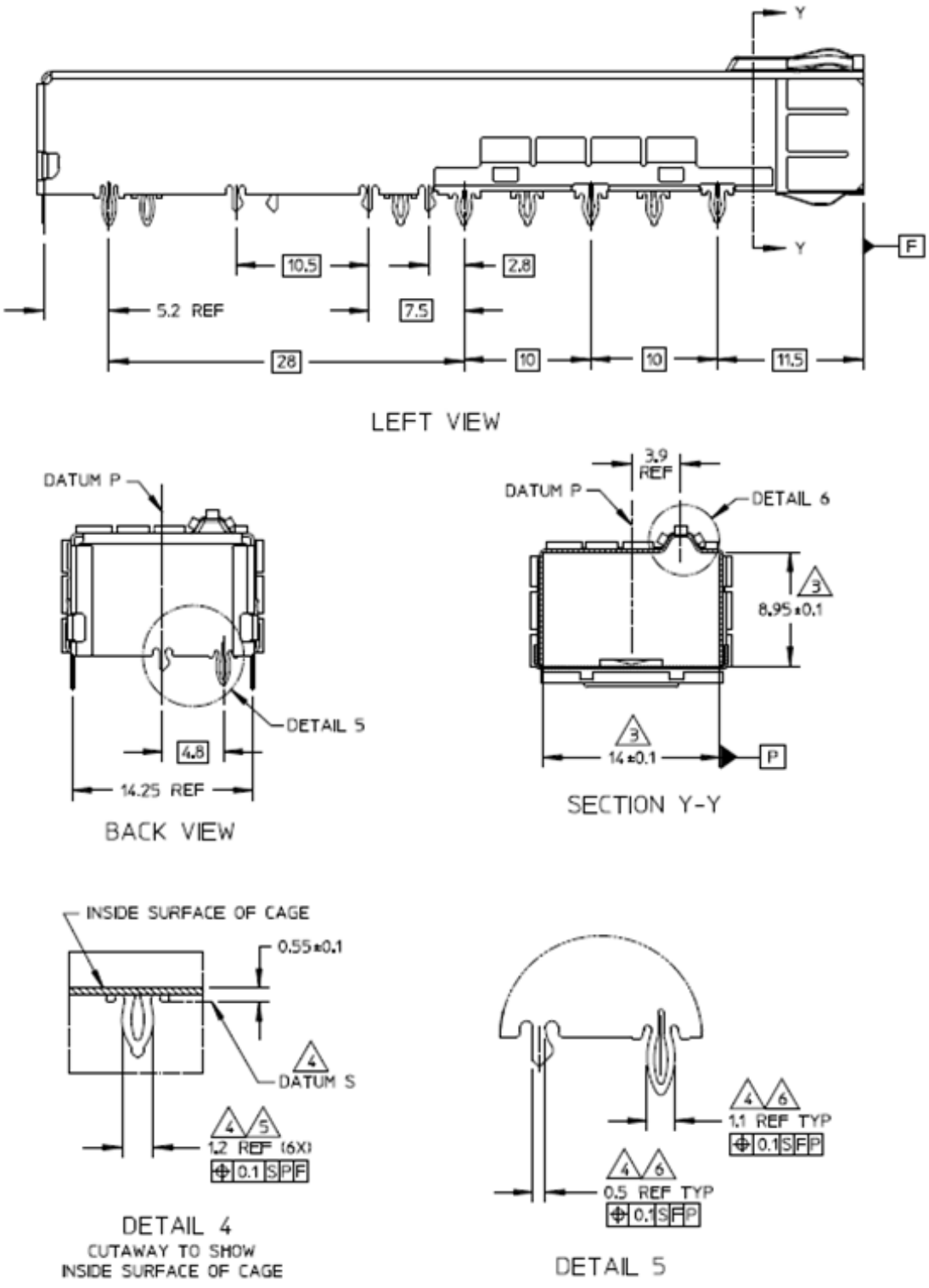


Figure 43: Press Fit 1x1 Cage Design

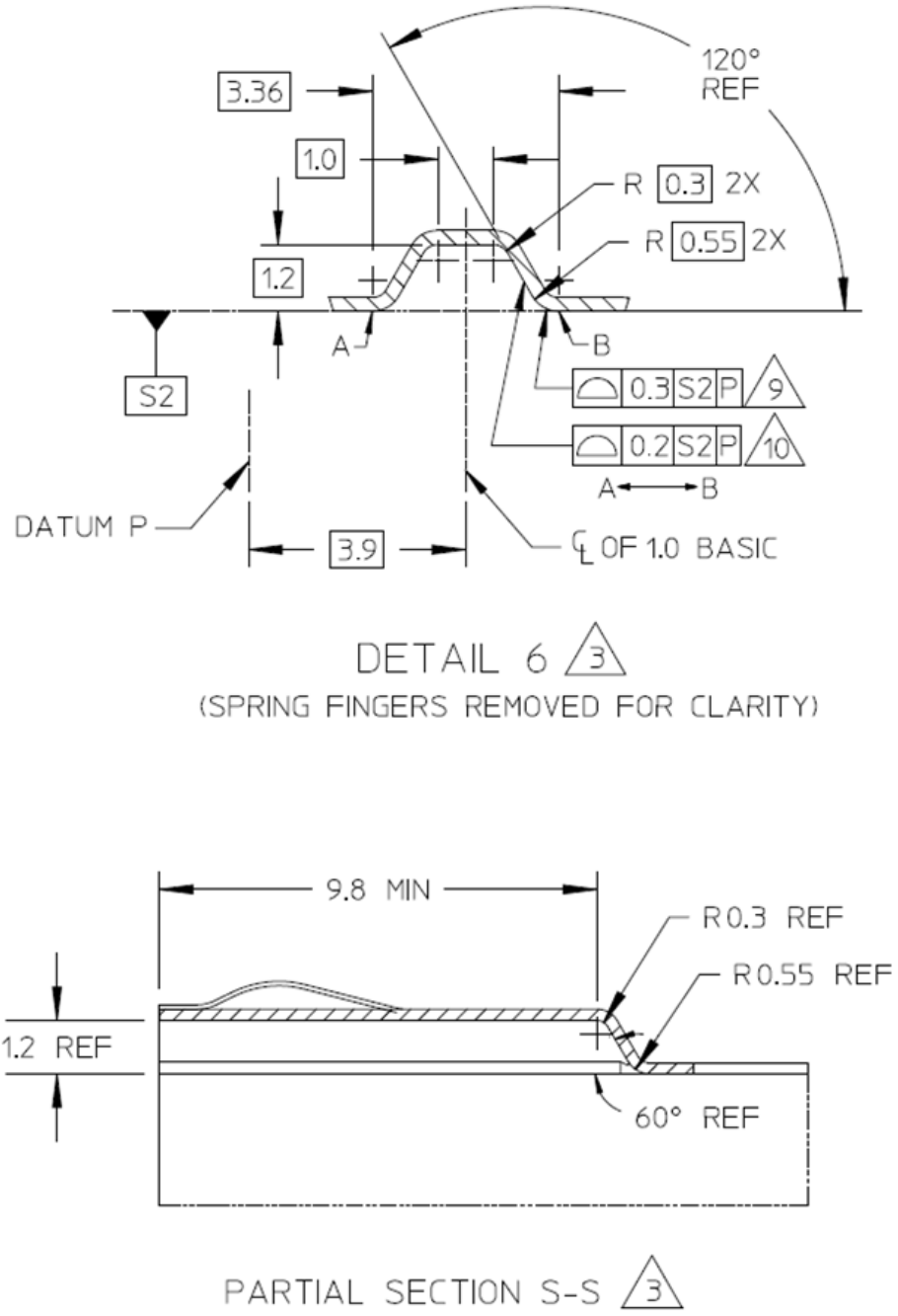


Figure 44: Press Fit Cage Detail

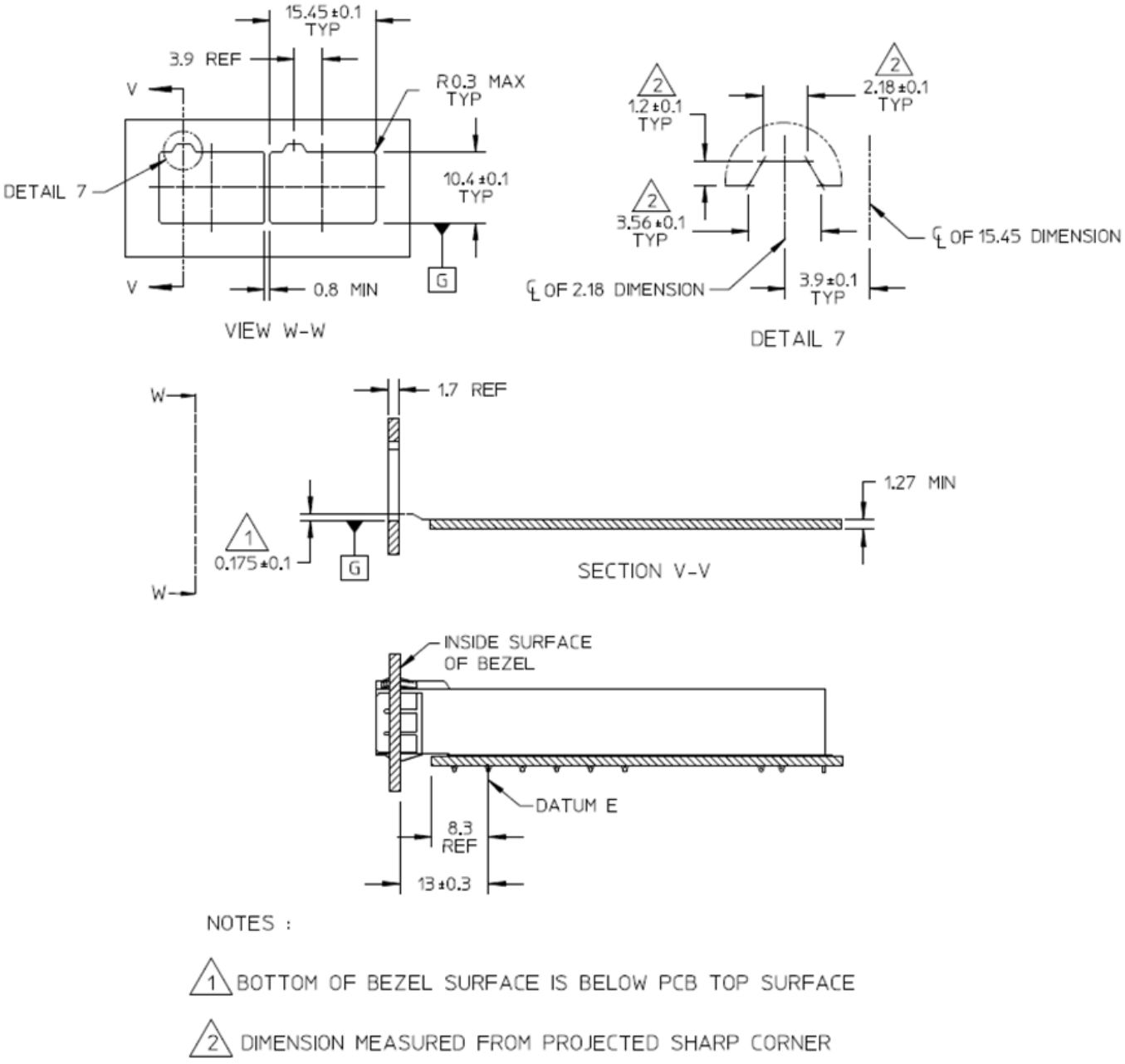


Figure 45: 1 x n bezel opening

7.9 SMT Electrical Connector Mechanical

The SFP-DD Connector is a 40-contact, right angle connector. The SMT connector is shown in Figure 46 with detailed drawings in Figure 47.

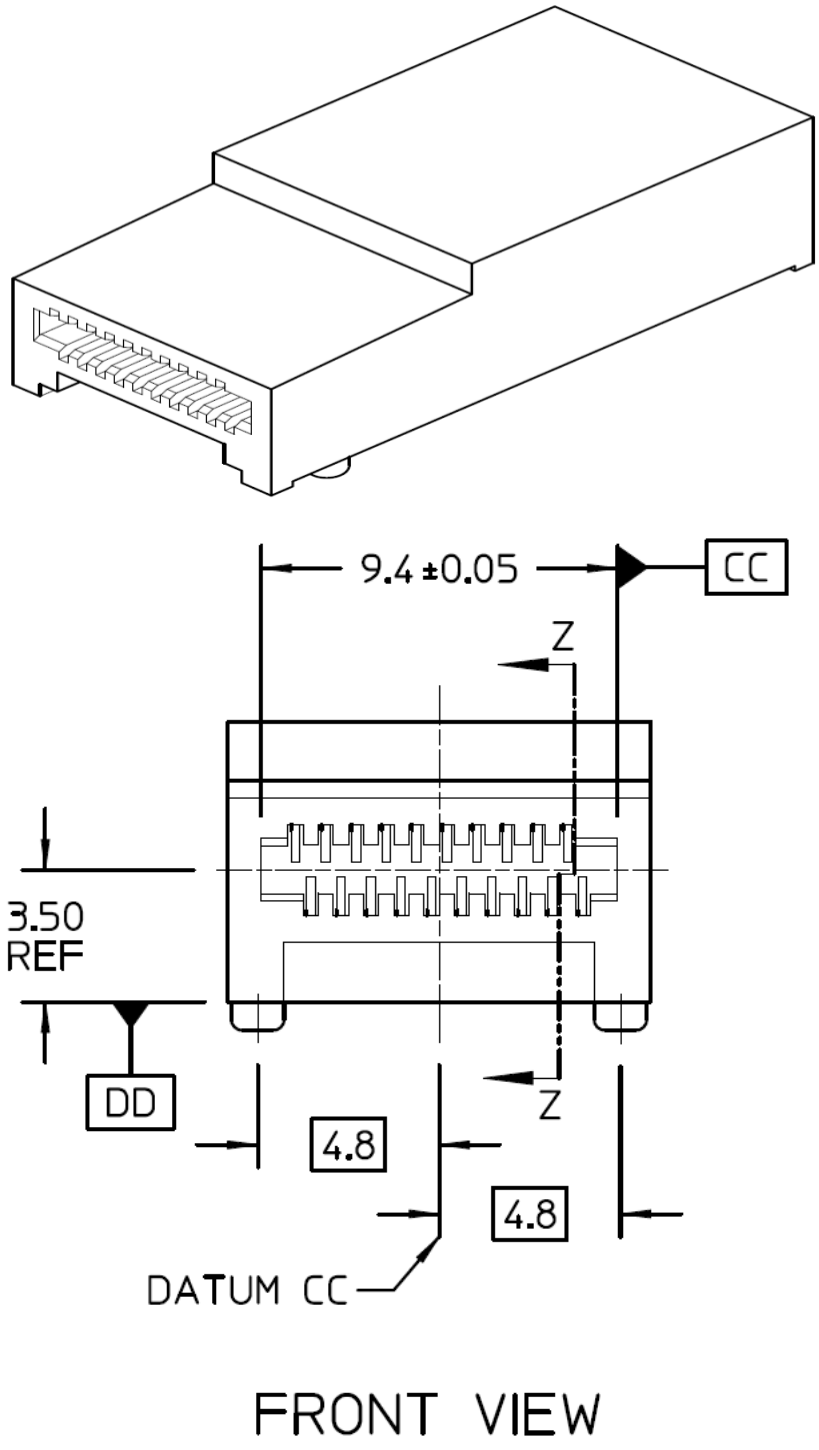
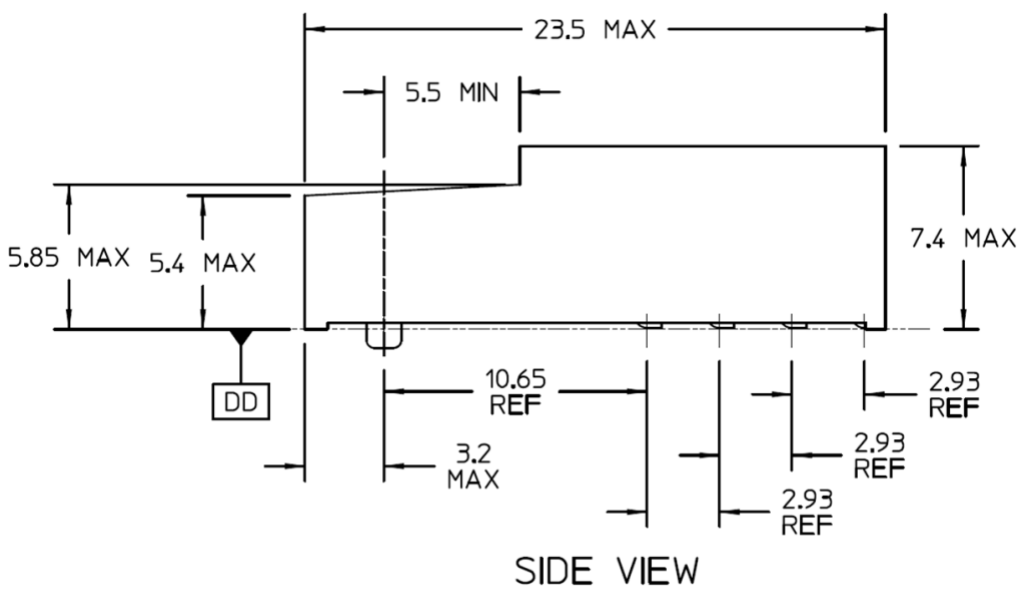
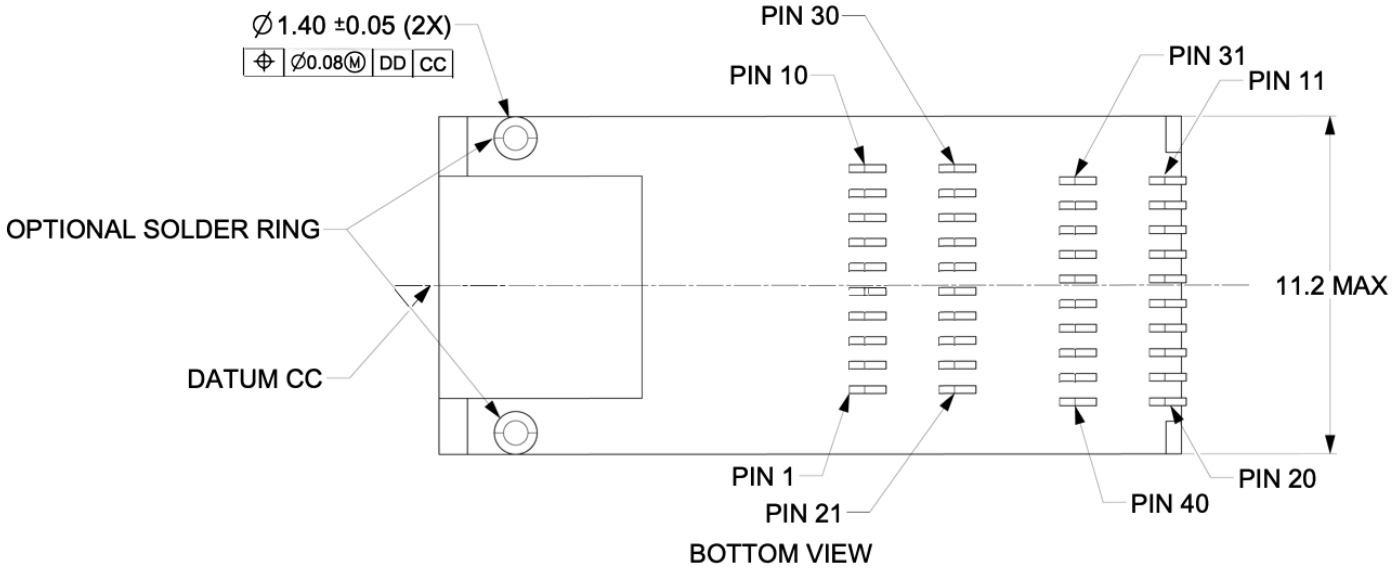


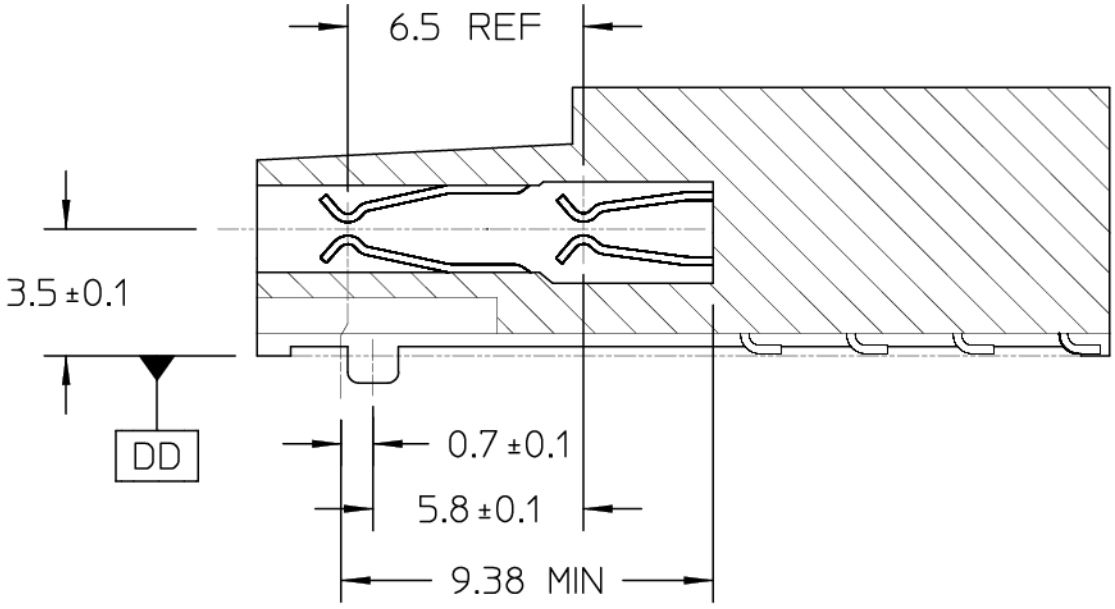
Figure 46: SMT connector


23.5 MAX
5.5 MIN
5.85 MAX
5.4 MAX
7.4 MAX
DD
10.65 REF
3.2 MAX
2.93 REF
2.93 REF
2.93 REF
SIDE VIEW

1
2


∅1.40 ±0.05 (2X)
∅0.08Ⓜ DD CC
PIN 30
PIN 10
PIN 31
PIN 11
OPTIONAL SOLDER RING
DATUM CC
11.2 MAX
PIN 1
PIN 21
PIN 40
PIN 20
BOTTOM VIEW

3



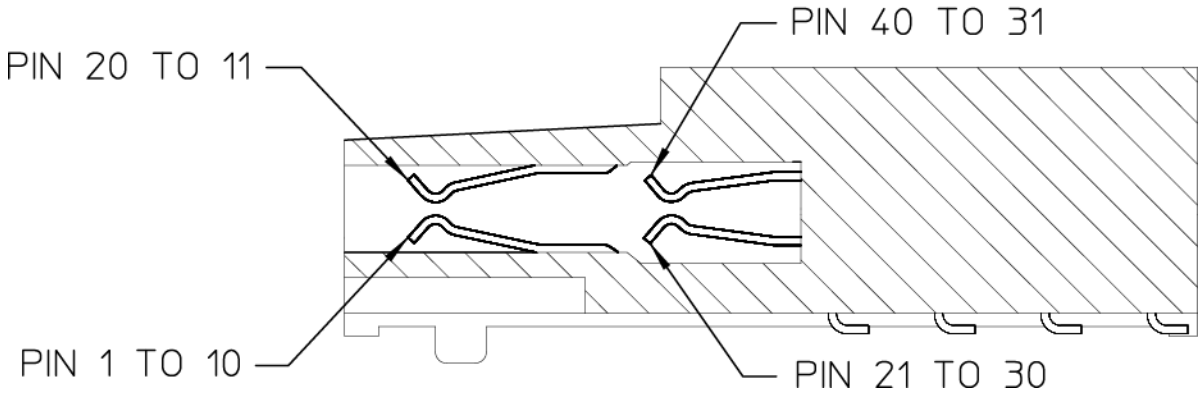
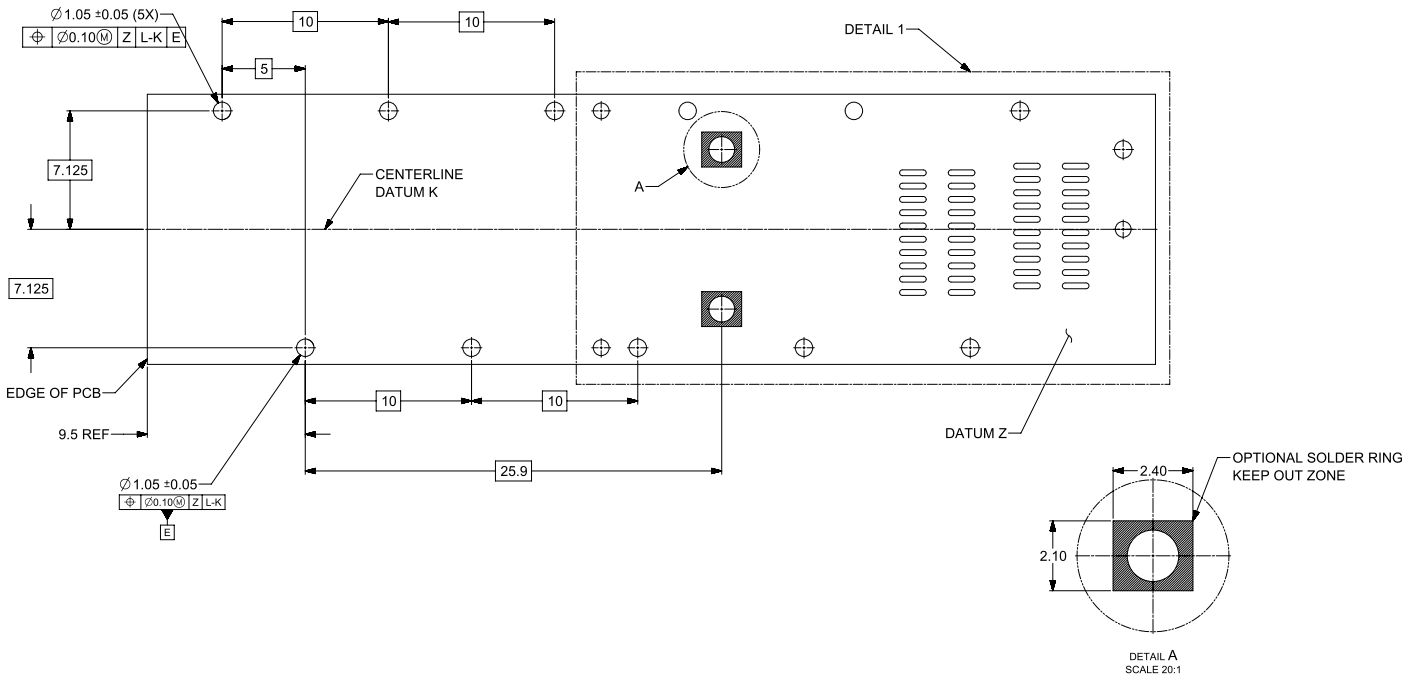


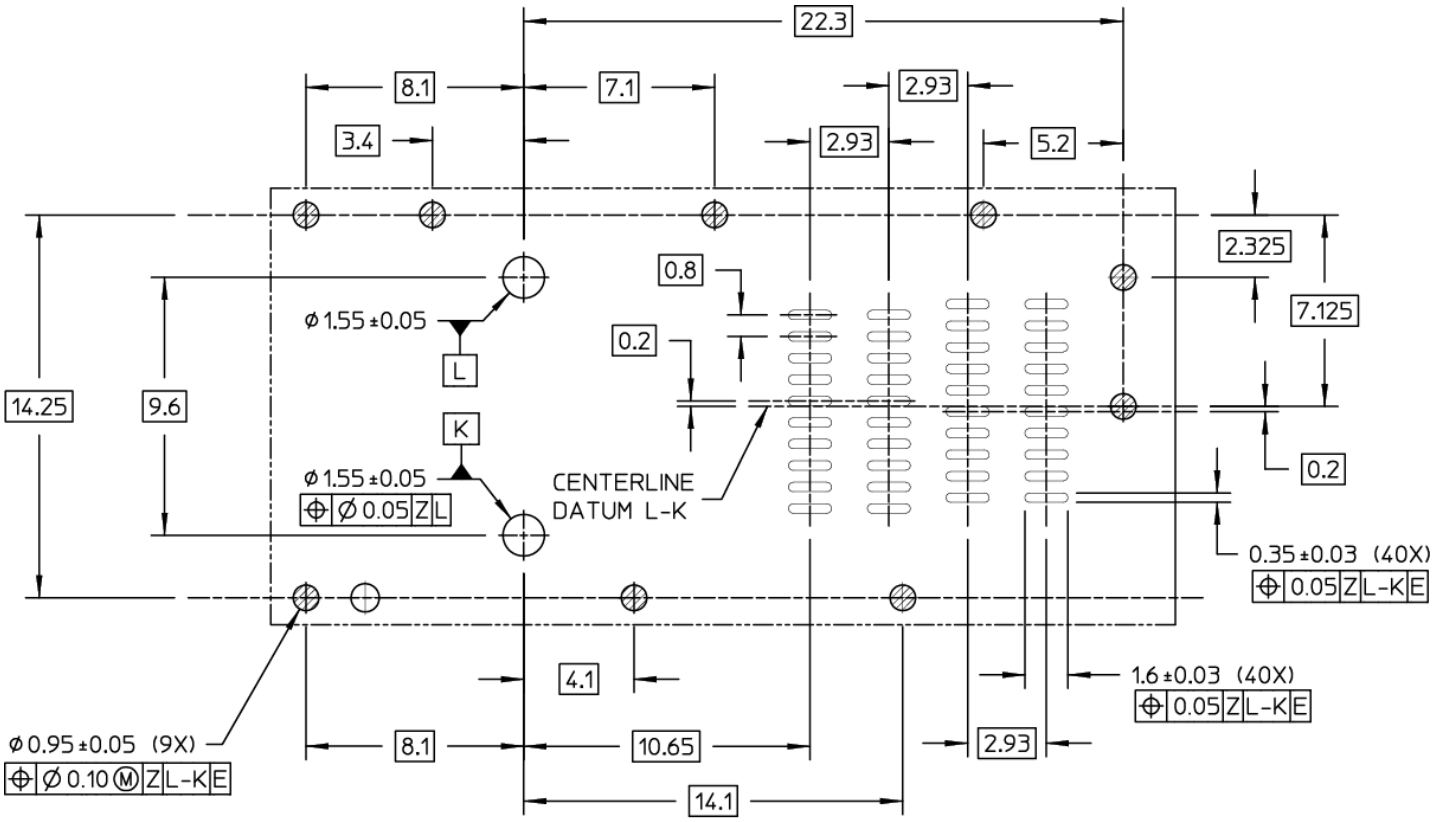
Figure 47: 1x1 Connector Design and Host PCB Pin Numbers

7.9.1 SMT connector and cage host PCB layout

A typical host board mechanical layout for attaching the SFP-DD SMT Connector and press fit Cage System is shown in Figure 48. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered, and attention paid to the host board layout.





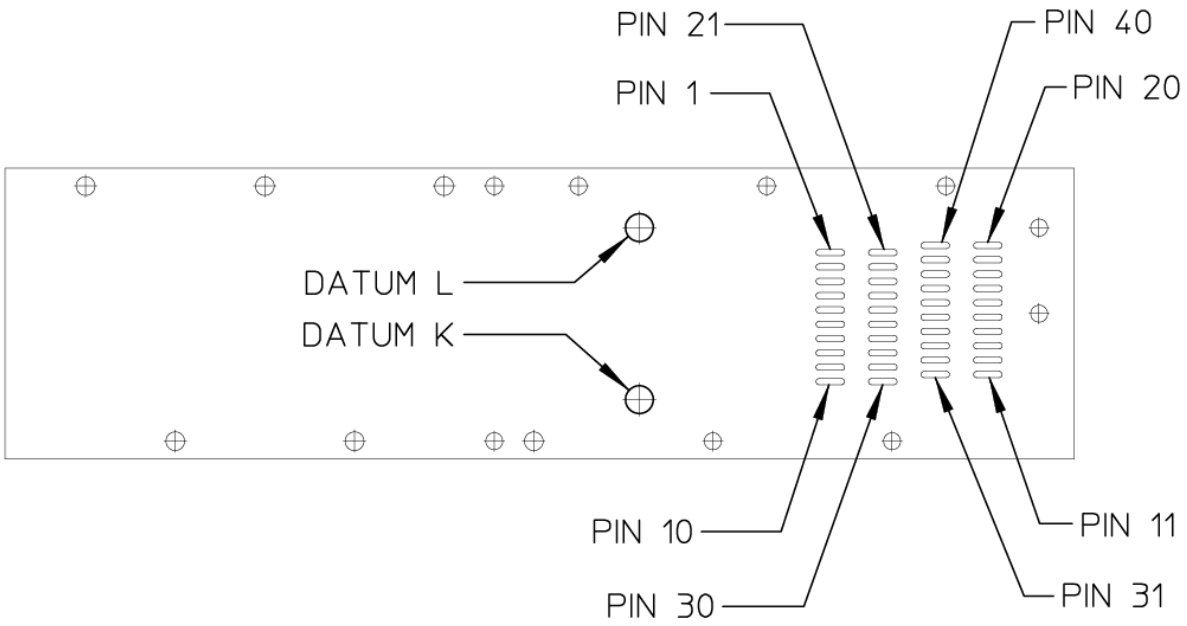


Figure 48: Host PCB Mechanical Layout

8. SFP-DD112 Mechanical and Board Definition

SFP-DD112 module mechanical specifications are compatible with SFP-DD module mechanical specifications in chapter 7, below are the list of relevant SFP-DD sections applicable to SFP-DD112:

- 7.1 Introduction to SFP-DD and SFP-DD112
- 7.2 SFP-DD/SFP-DD112/SFP112 Datums, Dimensions and Component Alignment
- 7.4 SFP-DD/SFP-DD112 Module Mechanical Dimensions
- 7.5 SFP-DD/SFP-DD112/SFP112 Module Flatness and Roughness
- 7.7 SFP-DD/SFP-DD112/SFP112 Module Extraction and Retention Forces.
-

8.1 Introduction

The module paddle card dimensions of the SFP-DD112 have been improved to support 100 Gb/s PAM4 (up to 56 GBd) serial data rates, see Section 4.

SFP-DD112 supports multiple connector/cage form factors. SFP-DD112 cages/connectors/modules are compatible with SFP-DD cages/connectors/modules, SFP-DD112 cages/connectors also accepts SFP+/SFP28 [30]/[28] family of modules. Examples of SFP-DD112 cages are:

- 1x1 surface mount connector/cage.

8.2 SFP-DD112 module mechanical dimensions

The mechanical outline for the SFP-DD112 module and direct attach cables are identical to Figure 22. The module shall provide a means to self-lock within the cage upon insertion. The module package dimensions are identical to Figure 23 with exception of bottom view shown in Figure 49. For SFP-DD112 modules the bottom surface of the module within the cage shall be flat without a pocket. The options for the position of the label could include the bottom surface of the module that protrudes outside the bezel of the cage or etched into the metal surface.

Caution should be exercised that any etchings do not affect thermal performance. Flatness and roughness specs are defined in 7.5 apply to both top and bottom surfaces of SFP-DD112 module.

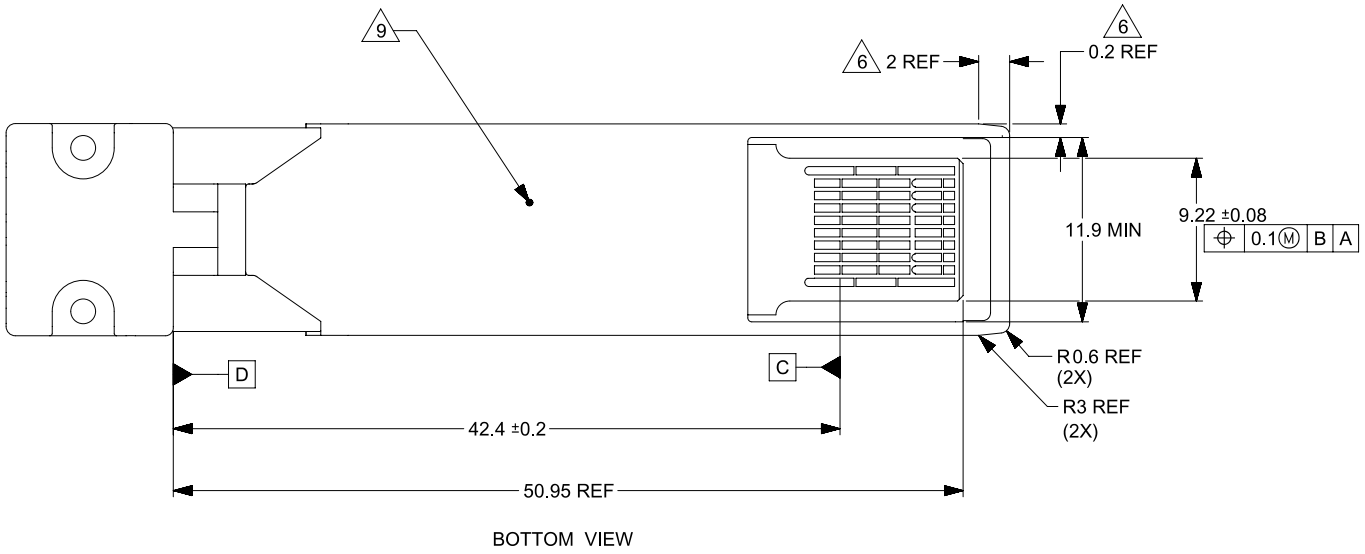


Figure 49: SFP-DD112 Module Bottom View Details

8.3 SFP-DD112 Improved Module paddle card dimensions

NOTES APPLY TO MODULE PADDLE CARD:

1. DIMENSIONS AND TOLERANCCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD

5 DATUM C IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTERMOST SIGNAL CONTACT PADS TO BE RE-ESTABLISHED ON EACH SIDE

6 DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS

7 DIMENSION AND TOLERANCE APPLIES TO ALL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

8 A ZERO GAP IS ALLOWED FOR A CONTINIOUS PAD OPTION

9 APPLIES TO ALL SIGNAL PAD TO PRE-WIPE SPACING

10 PRE-WIPE PADS (SHADED AREA), ON MODULE CARD HOST ARE REQUIRED

11 PRE-WIPE PADS (SHADED AREA), ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND DESIGNS

12 PRE-WIPE PADS (UNSHADED AREA), ARE REQUIRED EXCEPT IN CONTINUOUS POWER AND GROUND DESIGNS

13 PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS

14 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS

15 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS

16 COMPONENT KEEP OUT AREA MUST MEASURE FROM DATUM C

17 A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OG 0.13+/- 0.05 PRE-WIPE PADS ENSURE ADEQUATE WIPE REQUIRED TO PROVIDE A RELIABLE ELECTRICAL INTERCONNECT WHILE MINIMIZING SIGNAL INTEGRITY STUB EFFECTS

18 CONTACT PAD PLATING
0.38 MICROMETERS MINIMUM GOLD OVER
1.27 MICROMETERS MINIMUM NICKEL
ALTERNATE CONTACT PAD PLATING
0.05 MICROMETERS MINIMUM GOLD OVER
0.30 MICROMETERS MINIMUM PALLADIUM OVER
1.27 MICROMETERS MINIMUM NICKEL

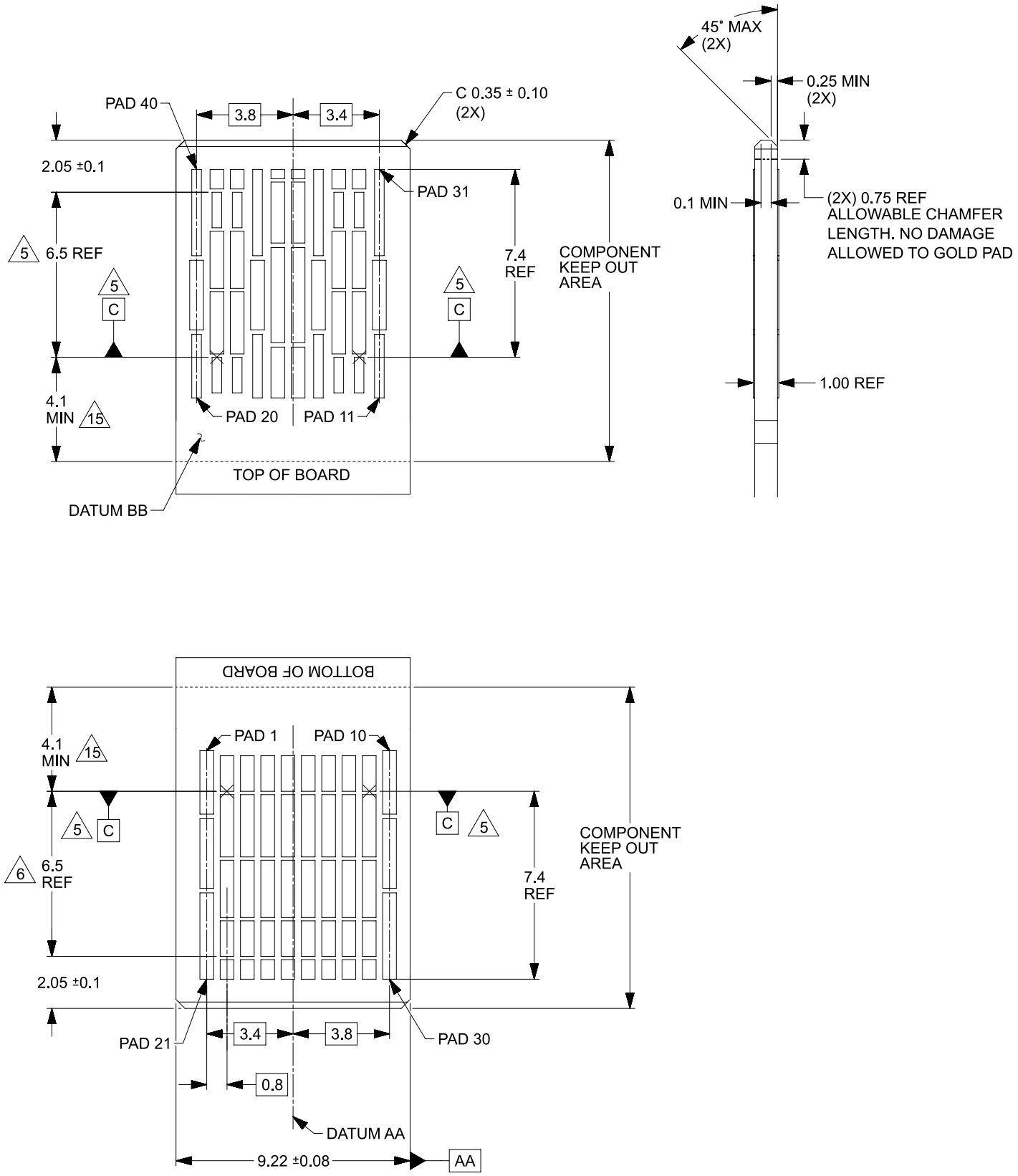


Figure 50: Improved module paddle card dimensions

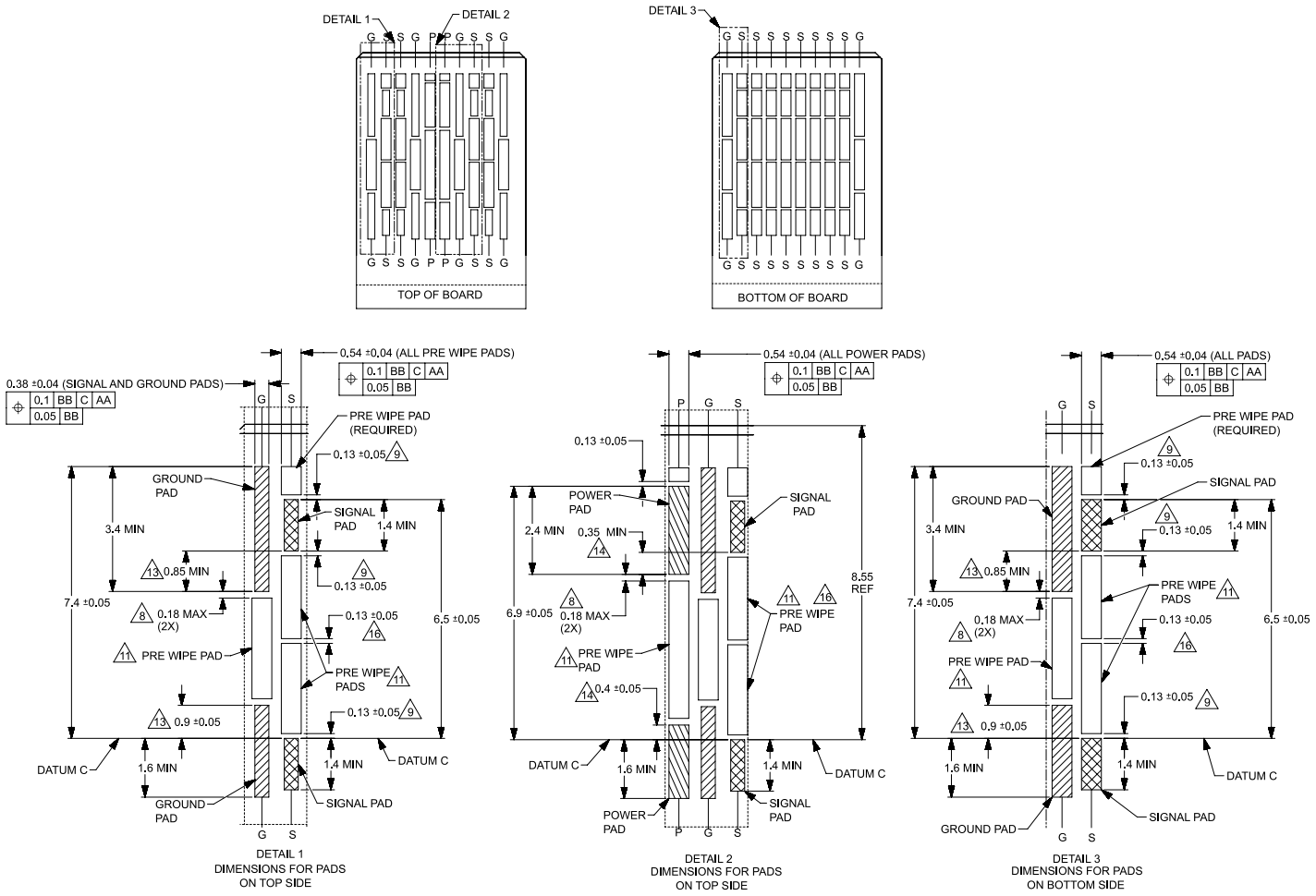


Figure 51: Improved module pad dimensions

8.4 Press fit Cage Mechanical

SFP-DD112 press fit cage is shown in Figure 52 with detailed drawings in Figure 43. SFP-DD112 cage bezel opening is identical to SFP-DD cage bezel as shown in Figure 45.

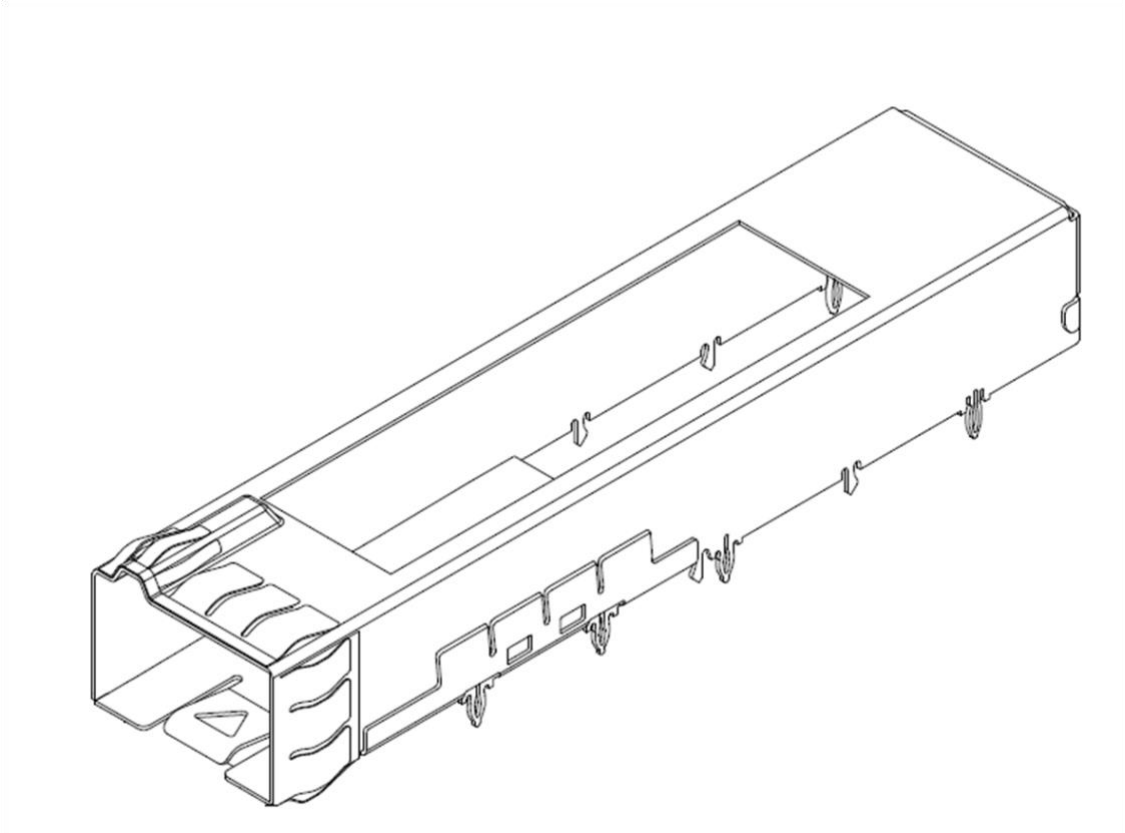
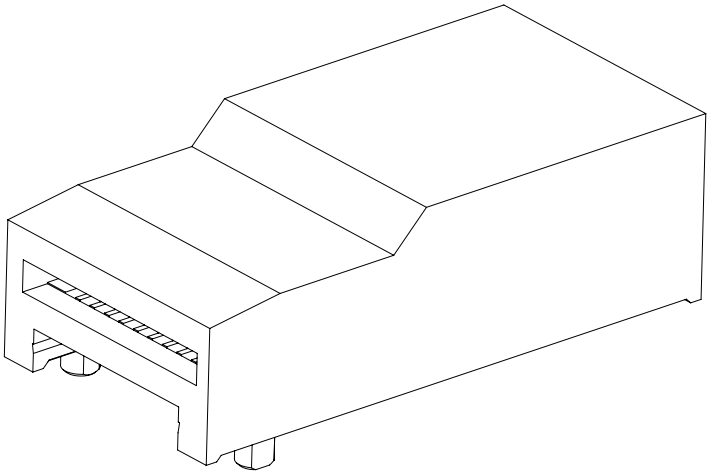
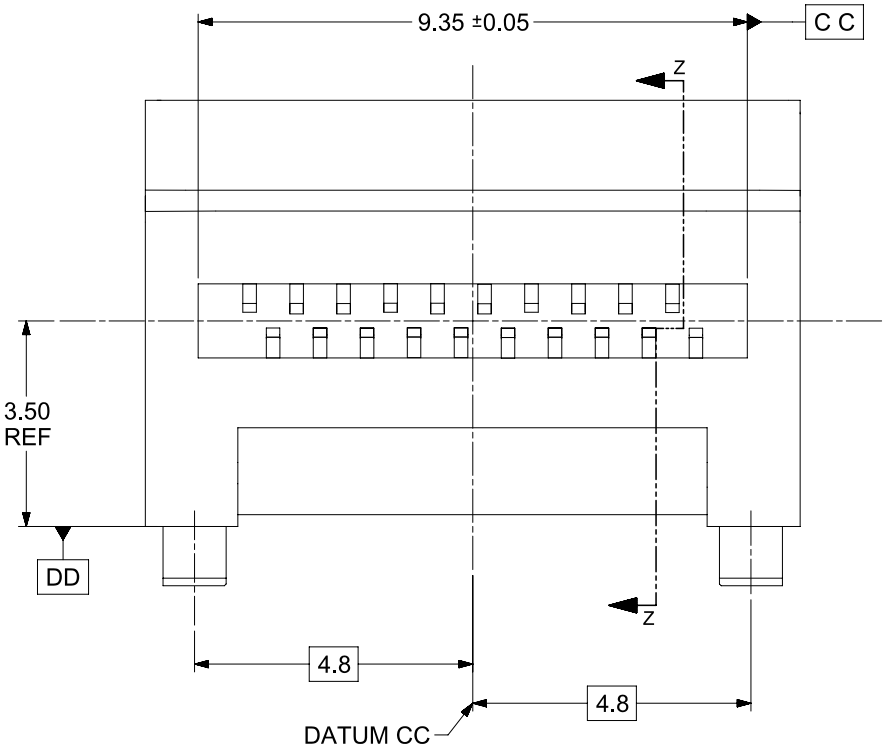


Figure 52: Press Fit 1x1 Cage

8.5 SMT Electrical Connector Mechanical

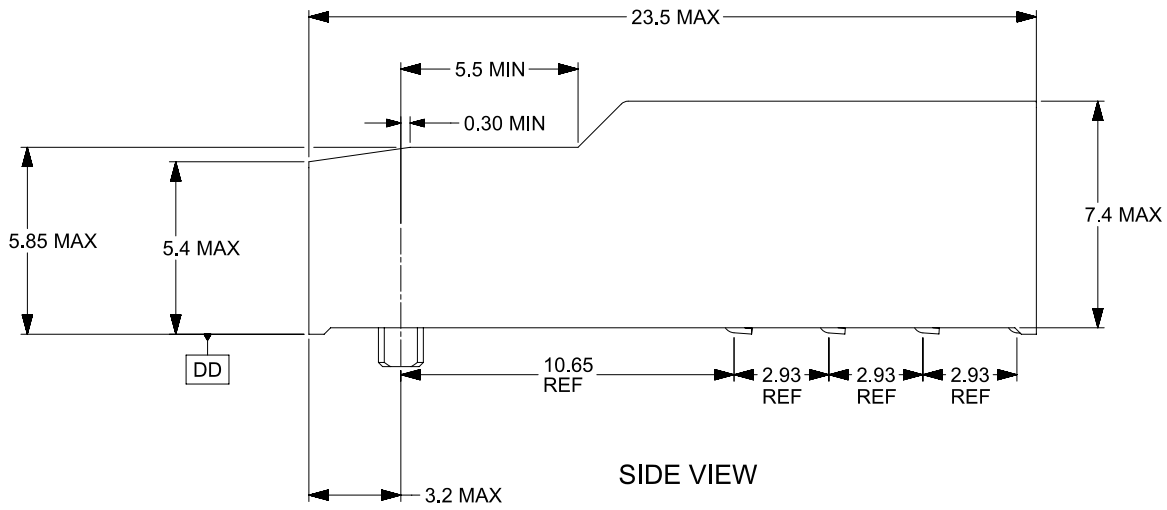
The SFP-DD112 Connector is a 40-contact, right angle connector. The SMT connector is shown in Figure 53 and connector/host PCB pinout shown in Figure 54.





FRONT VIEW

Figure 53: SMT connector



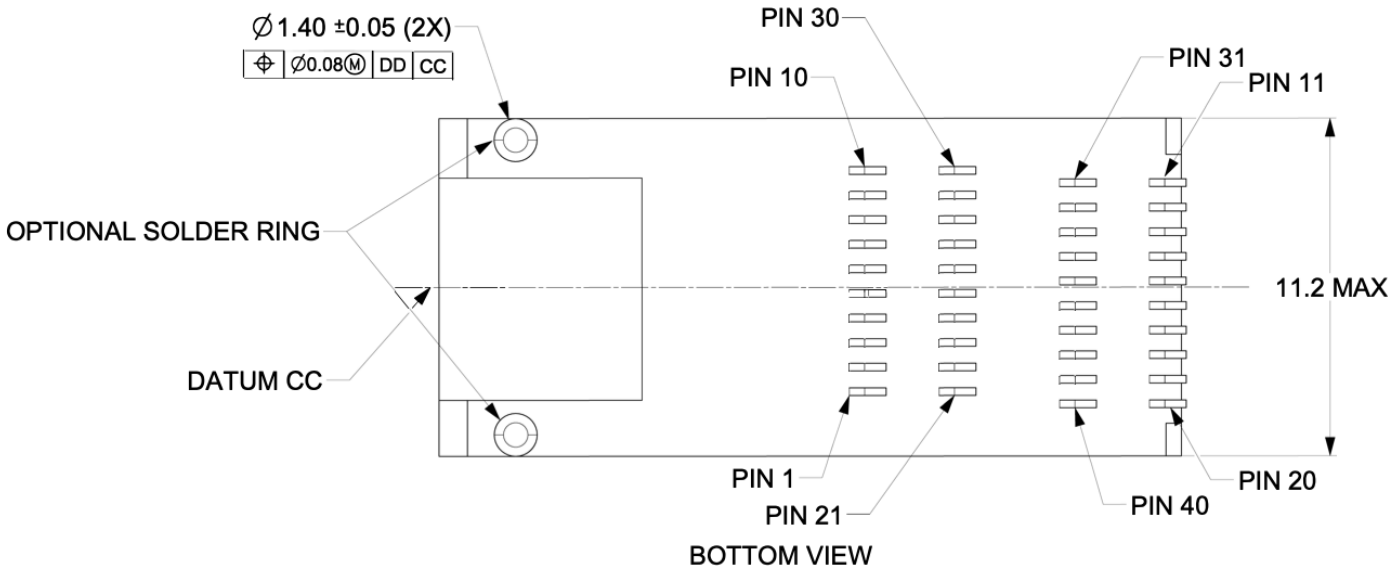
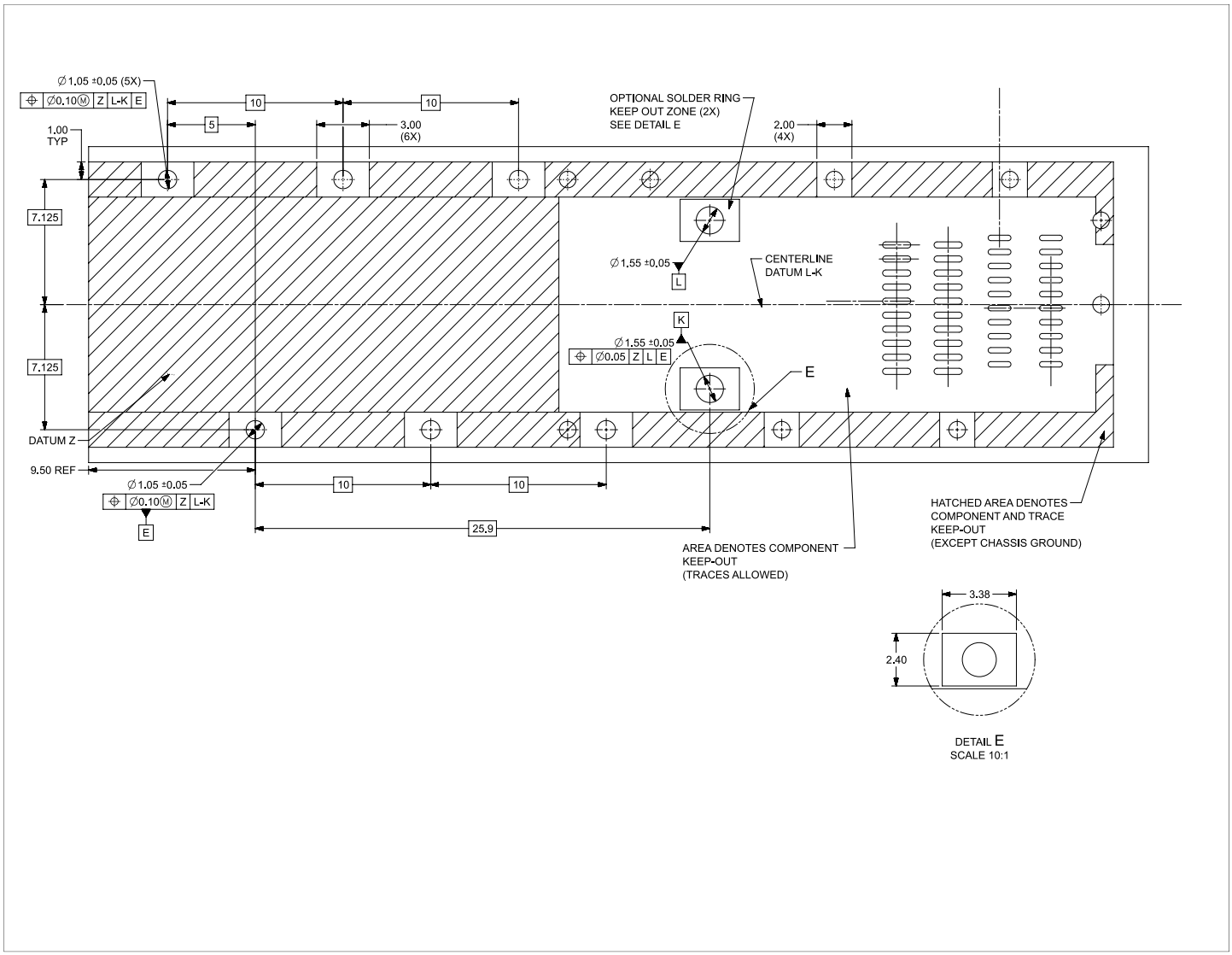


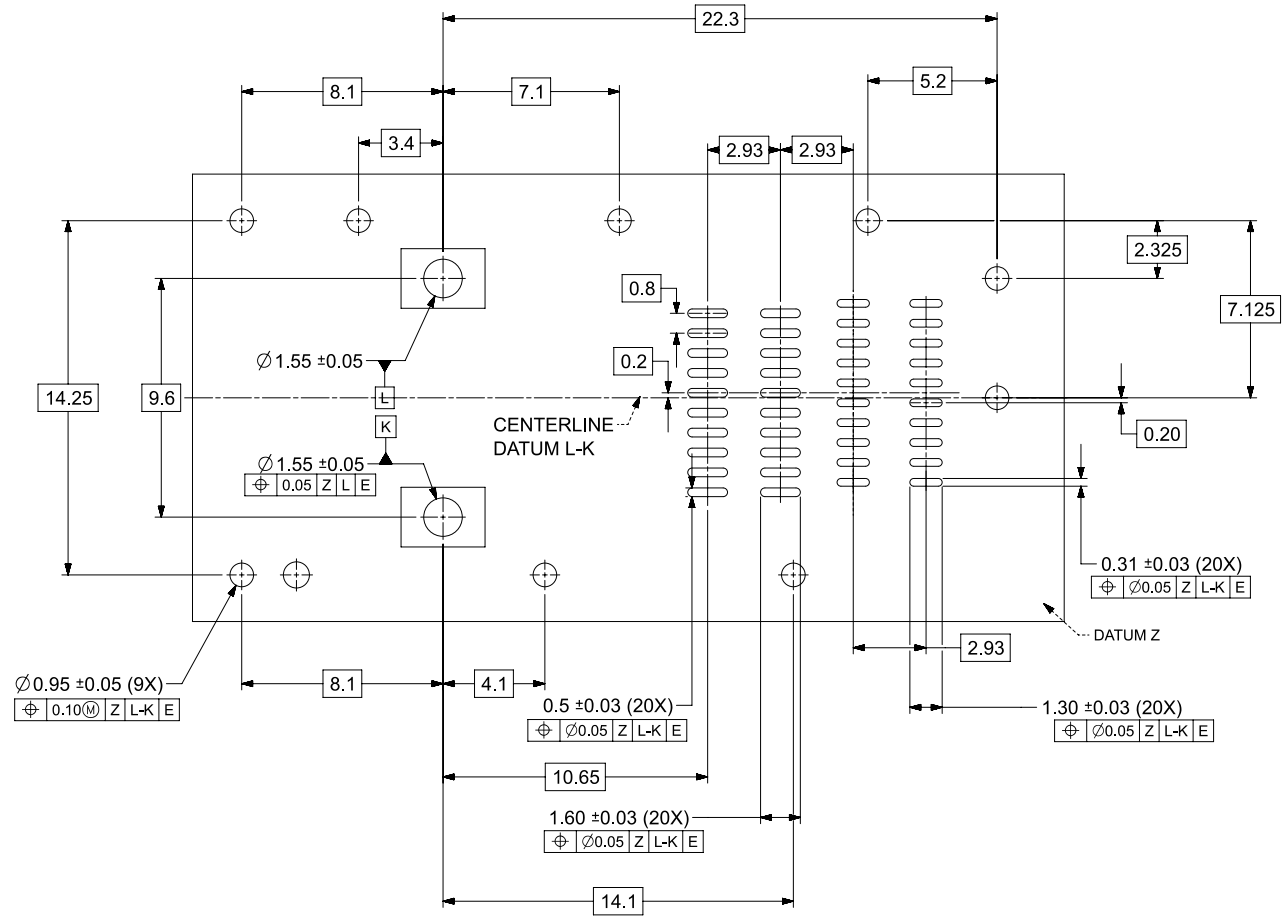
Figure 54: 1x1 Connector Design and Host PCB Pin Numbers

8.5.1 SMT connector and cage host PCB layout

A typical host board mechanical layout for attaching the SFP-DD112 SMT Connector and press fit Cage System is shown in Figure 48. Location of the pattern on the host board is application specific.

To achieve 112 Gbps (56 GBd) performance pad dimensions and associated tolerances must be adhered, and attention paid to the host board layout.





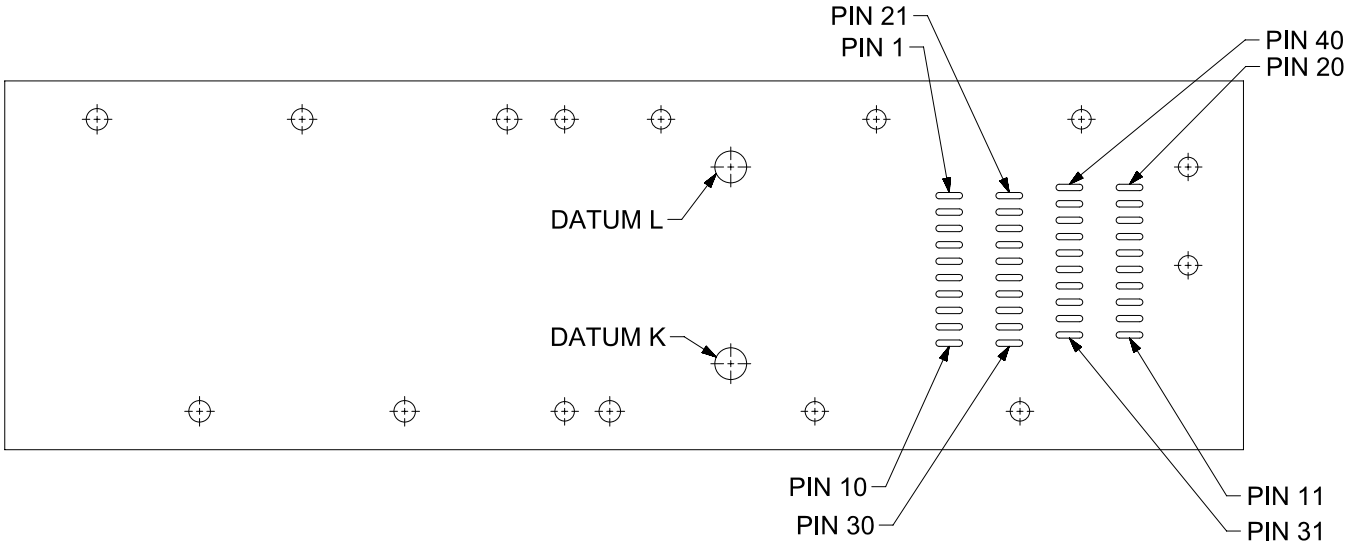


Figure 55: Host PCB Mechanical Layout

9. SFP112 Mechanical and Board Definition

SFP112 module mechanical specifications are compatible with SFP+/SFP28 [30]/[28]module mechanical specifications. Below are the list of relevant SFP+/SFP28 and SFP-DD sections applicable to SFP112:

- IPF General descriptions, [31][31] Chapter 3.0
- IPF Modules Dimensions, Retention/Extraction, and Durability, [31] Chapter 4
- IPF Cage Requirements, [31], Chapter 5
- SFP Single Cage Host Board Mechanical Layout, [26] Chapter 4A
- SFP+ Canged Cage Host Board Mechanical Layout, [32] Chapter 4
- SFP-DD/SFP-DD112/SFP112 Module Flatness and Roughness, 7.5
- SFP-DD/SFP-DD112/SFP112 Module Extraction and Retention Forces, 7.7.

9.1 Introduction

The module paddle card dimensions of the SFP112 have been improved to support 100 Gb/s PAM4 (up to 56 GBd) serial data rates compared to SFP+/SFP [30]/[28].

SFP112 supports multiple connector/cage form factors. All combinations of cages/connectors defined in the specification are backwards compatible to accept classic SFP28 and SFP+ modules. In addition, SFP112 modules are compatible with SFP28/SFP+ hosts for operation at lower speed.

9.2 SFP112 Datum for Module, Cage, Connector and Host

A listing of the SFP112 datums for the various components are contained in Table 27. To reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009 [4]. All dimensions are in millimeters.

Table 27: SFP112 Datum

Datum	Description
A	Center line of connector slot
B	Bottom surface of connector
C	Round guide-post of connector
D	Leading edge of signal contact pads on module paddle card
E	Leading edge of low speed contact pads on module paddle card
F	Front edge of module paddle card
G	Top surface of module paddle card
H	Center line of module paddle card width
K	Host board thru hole #1 to accept connector guide-post
L	Host board thru hole #2 to accept connector guide-post
M	Vertical center line of Datum L and Datum K
N	Top surface of host board
P	Hard stop on module
R	Hard stop on cage
S	Host board thru hole to accept primary cage press fit pin
T	Center line of module width
U	Bottom surface of module

9.3 SFP112 Cage, Connector, Module Alignment

The alignment of the cage, connector and module are shown in Figure 56.

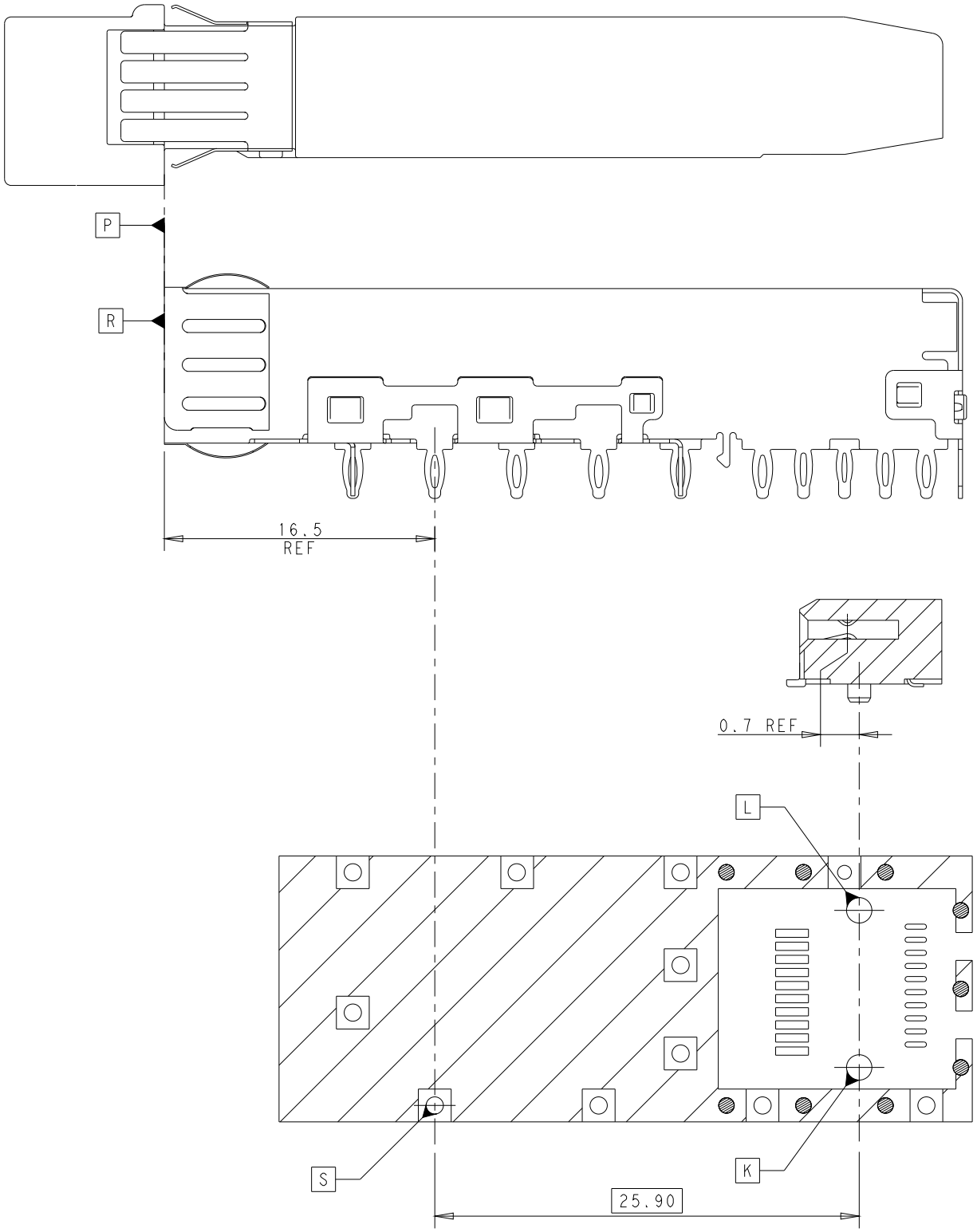


Figure 56: SFP112 1x1 Cage and Host PCB Layout

9.4 SFP112 module mechanical dimensions

SFP112 modules mechanical dimension are identical to SFP+/SFP28 [30]/[28] modules with exception of viewing windows to inspect high speed pad as shown Figure 57. A SFP28/56 [28] cage can be used with the SFP112 connector. For SFP112 modules the bottom surface of the module within the cage shall be flat without a pocket. The options for the position and the bottom view of the label could include the bottom surface of the module that protrudes outside the bezel of the cage or etched into the metal surface. Caution should be exercised that any etchings do not affect thermal performance.

Flatness and roughness specs are defined in 7.5 to both top and bottom surfaces of SFP112 module.

NOTES APPLY TO MODULE DRAWINGS:

NOTES APPLY TO MODULE DRAWINGS:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y145−2009.
2. SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS
3. RECOMMENDED MAXIMUM MODULE LENGTH EXTENDING OUTSIDE OF CAGE. OTHER LENGTHS ARE APPLICATION SPECIFIC.
4. INDICATED OUTLINE DEFINES MAXIMUM ENVELOP OUTSIDE THE CAGE.
   THE SURFACES OF THE MAXIMUM ENVELOP MAY BE CONTACTED BY AN ADJACENT MODULE EMI SPRINGS DURING INSERTION AND EXTRACTION OF THE MODULE FROM THE CAGE. THE SURFACES SHALL NOT HAVE ANY SHAPES OR MATERIALS THAT CAN DAMAGE THE ADJACENT MODULE EMI SPRINGS OR BE DAMAGED THEMSELVES BY THE SPRINGS.
5. DMENSIONS DEFINES EMI SPRING CONTACT PONT WITH MODULE CAGE.
6. FLATNESS SPECIFICATION APPLIES OVER THE ENTIRE HEAT SINK AREA REFER TO SECTION 5.4 TABLE 6 FOR FLATNESS REQUIREMENTS.
7. PRODUCT LABEL ON BOTTOM AND/OR SIDES TO BE FLUSHED OR RECESSED BELOW EXTERNAL SURFACES. LABEL(S) SHALL NOT INTERFERE WITH THE MECHANICAL, THERMAL, OR EMC PROPERTIES.

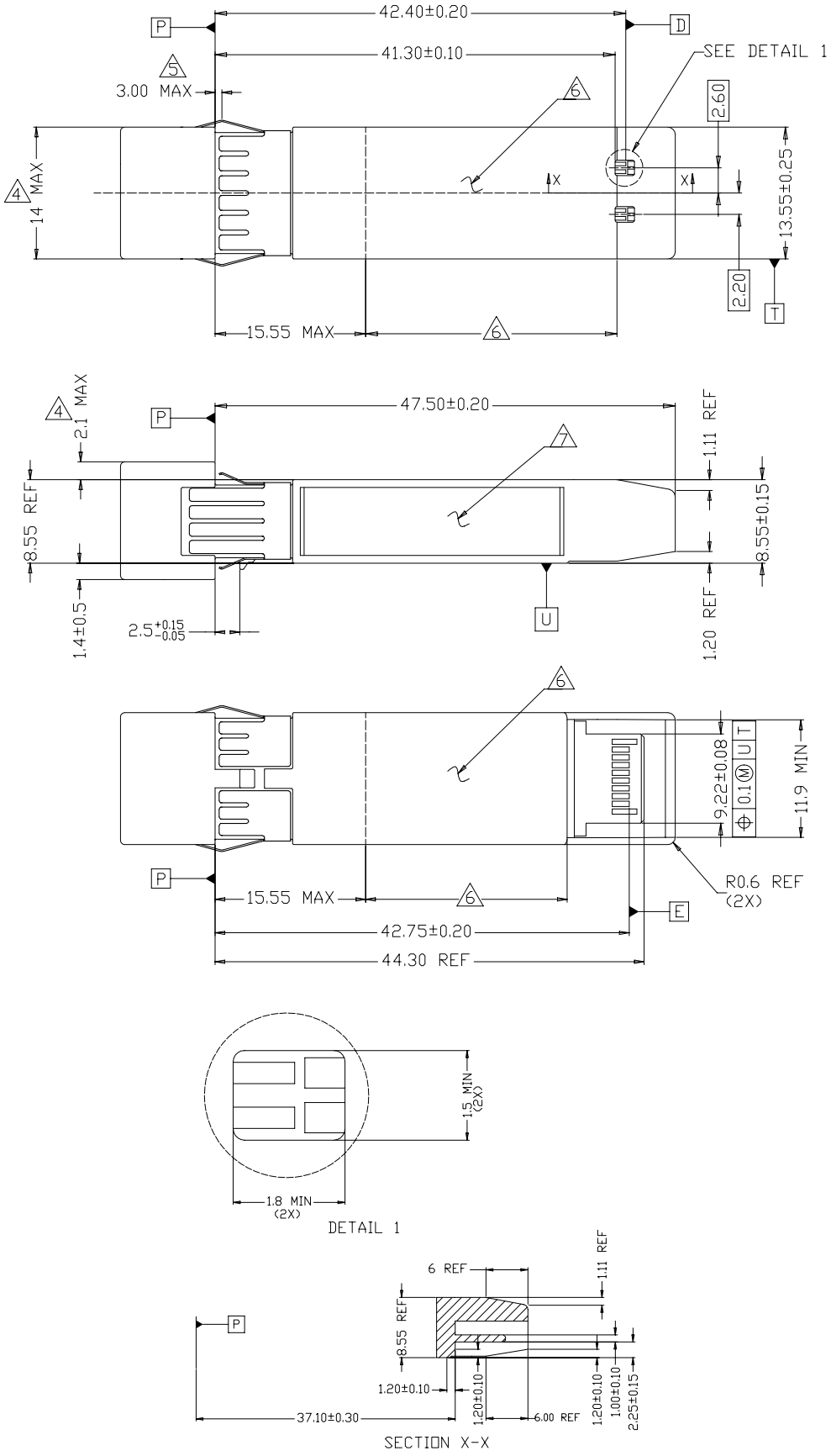


Figure 57: SFP112 High Speed Pads Viewing Windows

9.5 SFP112 Improved Module paddle card dimensions

The SFP112 module paddle card pad dimensions have been modified to support 112 Gb/s (56 GBd) serial data rates. SFP112 module paddle card pad dimensions optimized for 56 GBd operation shown in Figure 58. All other module dimensions, except for the pads are the same as the SFP+/SFP28 [30]/[28] specifications.

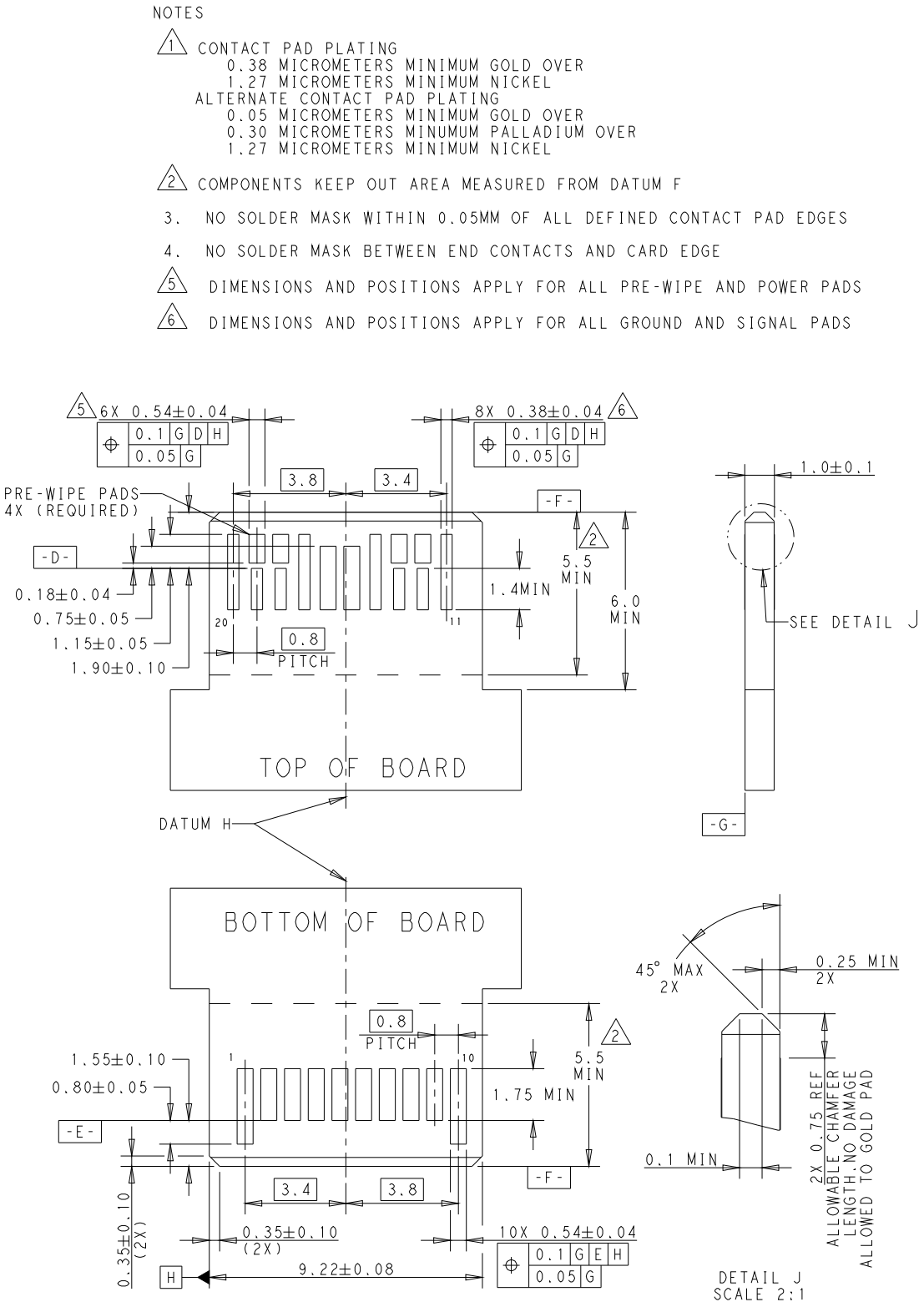


Figure 58: SFP112 improved module paddle card dimensions

9.6 SFP112 SMT Electrical Connector

The SFP112 Connector is a 20-contact improved right-angle connector compatible with SFP+ modules [31]. The SFP112 SMT connector is shown in Figure 59.

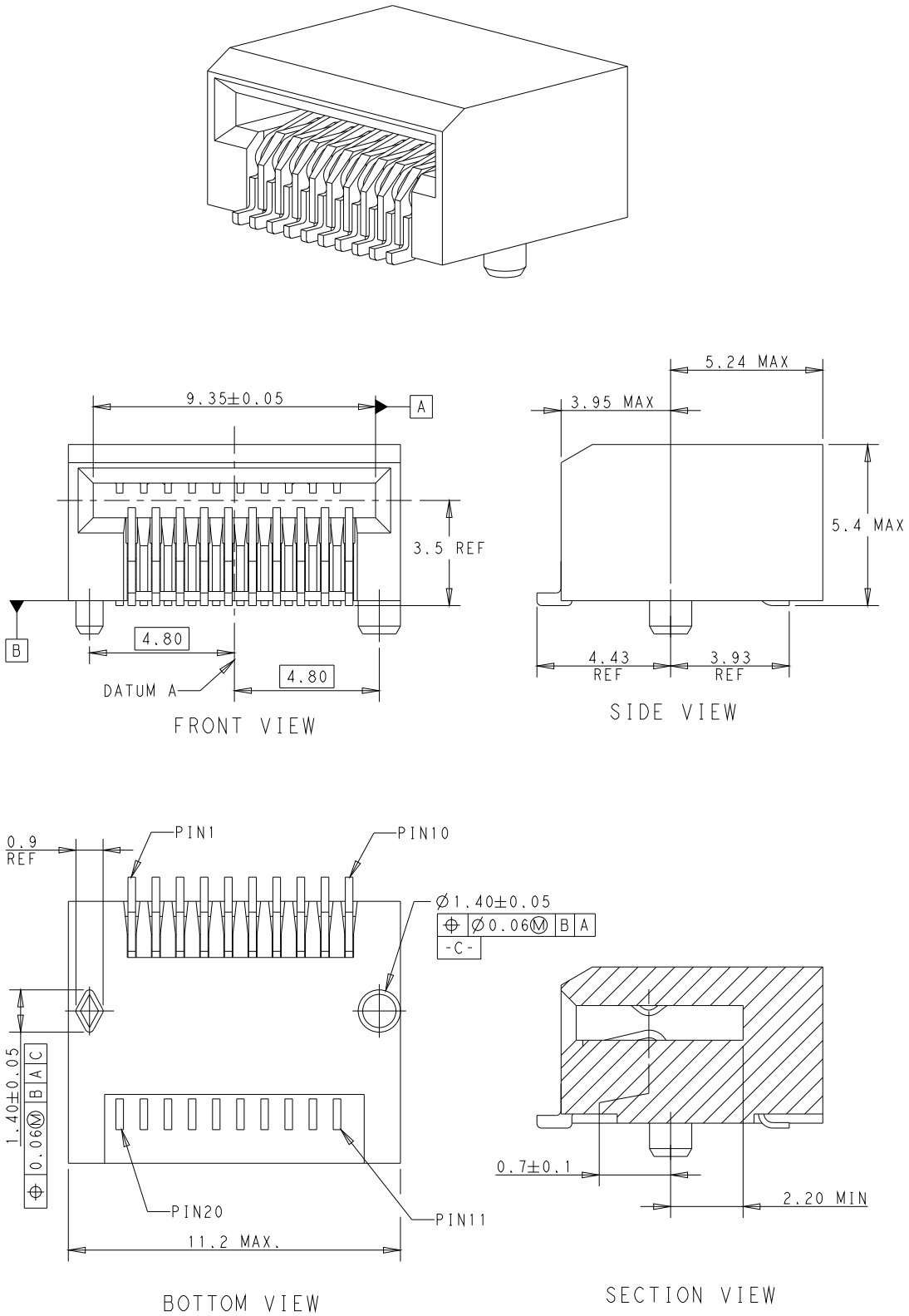


Figure 59: SFP112 SMT Connector

9.6.1 SFP112 SMT host PCB layout

A typical host board mechanical layout for attaching the SFP112 surface mount Connector is shown in Figure 60. The detailed optimized SFP112 host pad layout is shown in Figure 60 and the host PCB pad numbers shown in Figure 62. Note: the cage footprint for SFP112 is the same the same as SFP cage footprint, [26] see Figure 4A.

To achieve 112 Gbps (56 GBd) operation the SFP112 pad dimensions and associated tolerances have improved compared to SFP+/SFP28 [30]/[28] as shown in Figure 61. One must adhere and pay attention to the host board layout for 56 GBd operation.

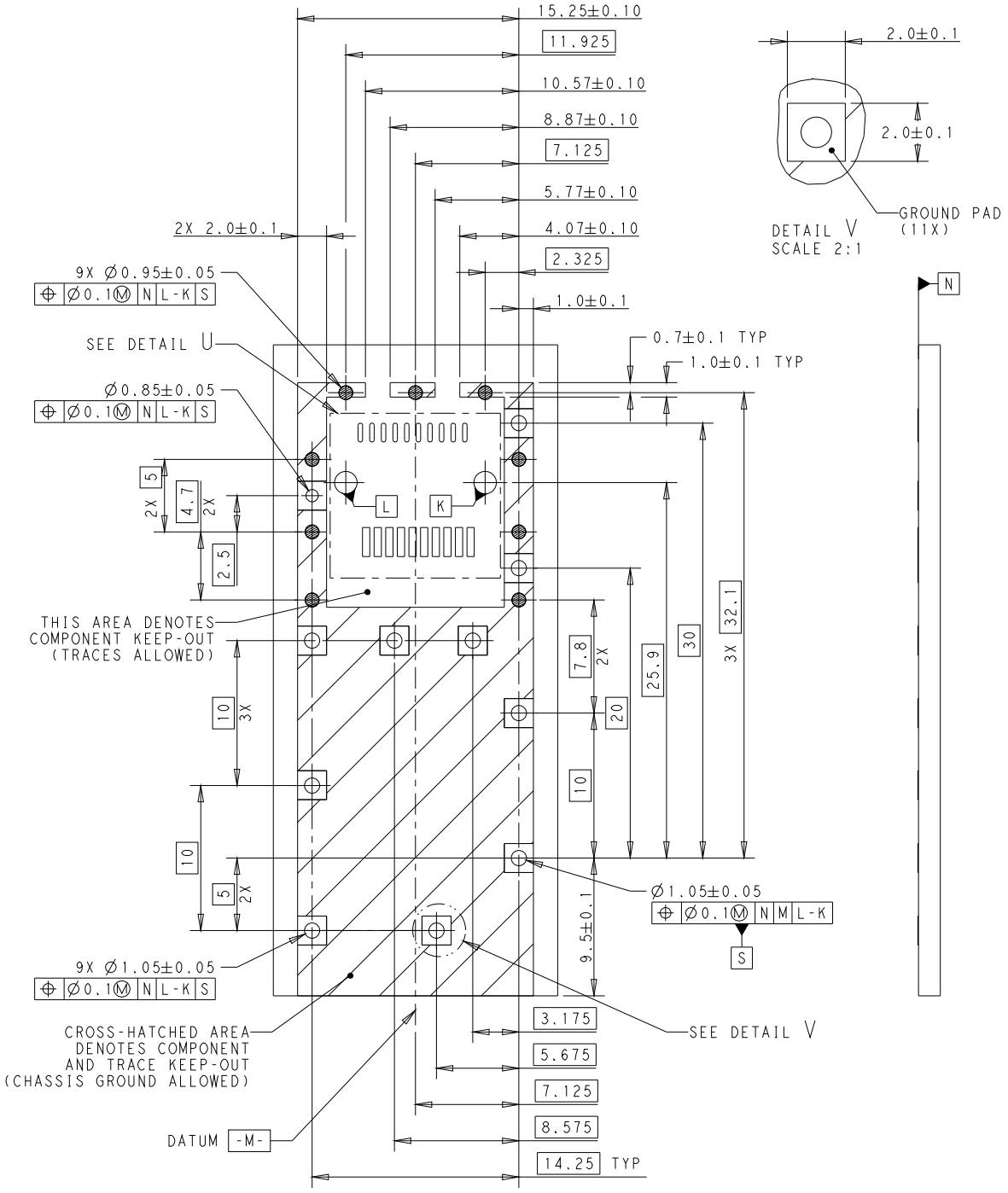


Figure 60: SFP112 Host Pad Layout

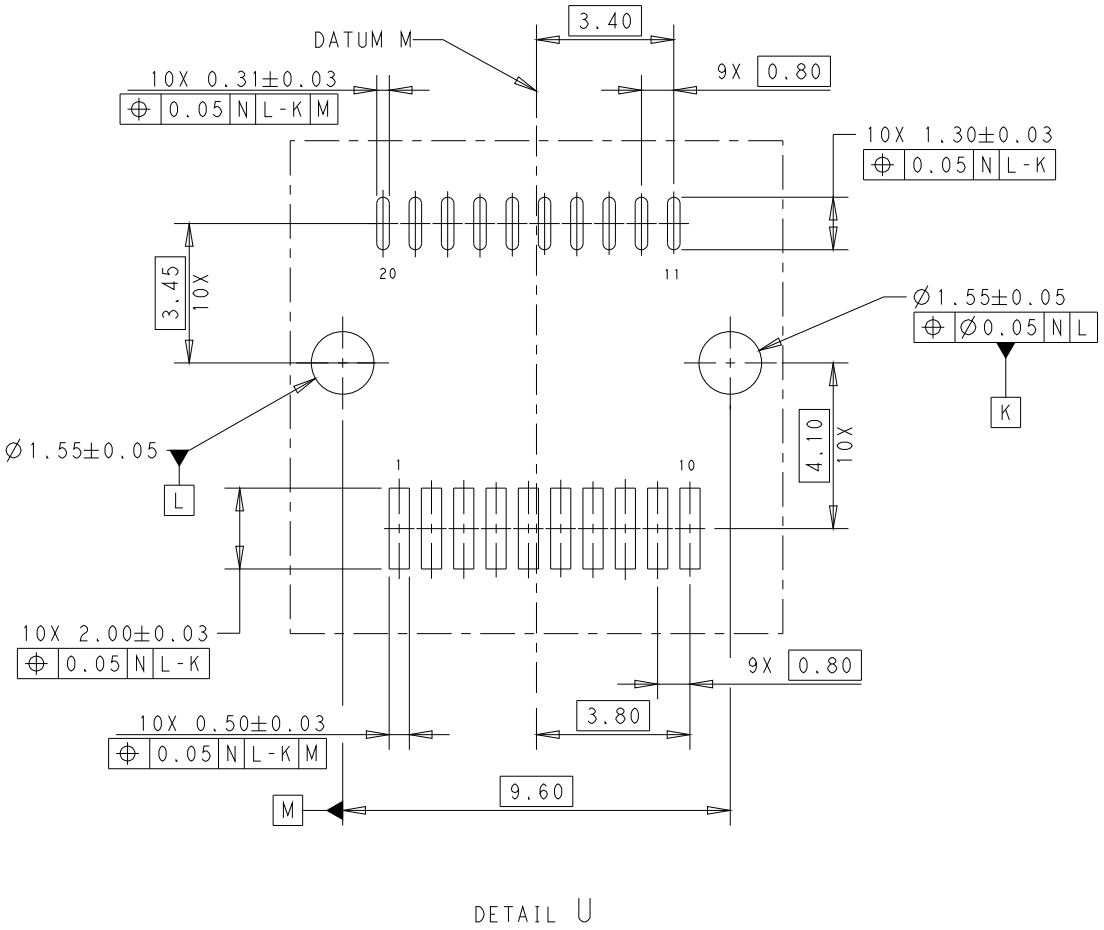


Figure 61: SFP112 Detailed Host Pad Layout

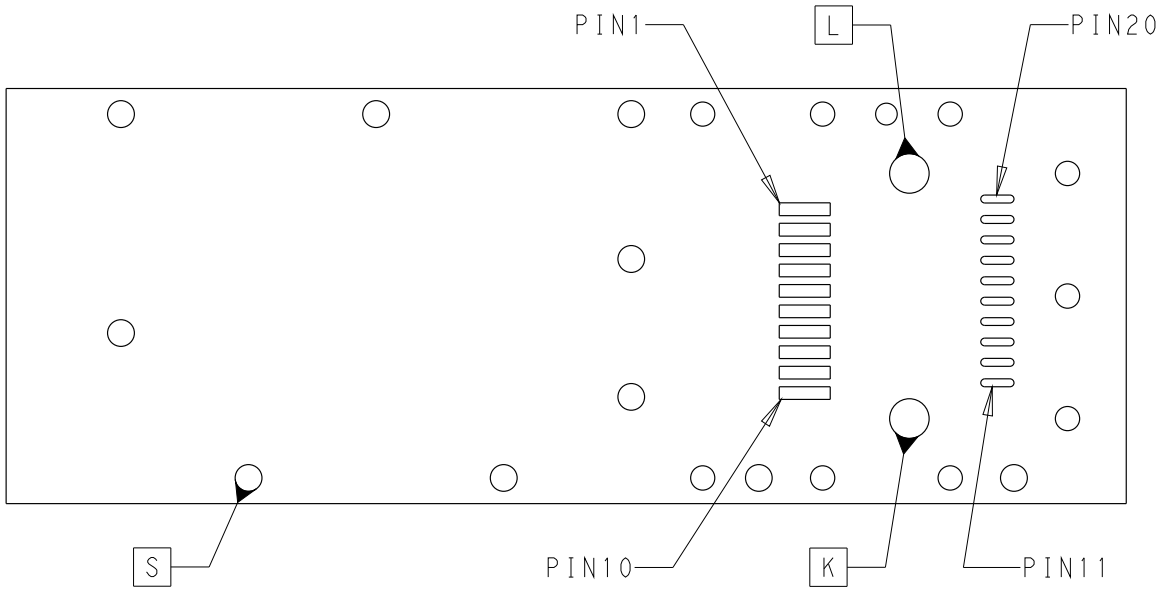


Figure 62: 1x1 Connector Design and Host PCB Pad Numbers

10. Environmental and Thermal

10.1 Thermal Requirements

The SFP-DD/SFP-DD112/SFP112 module shall operate within one or more of the case temperatures ranges defined in Table 28. The temperature ranges are applicable between 60 m below sea level and 1800 m above sea level, NEBS GR-63 [18], utilizing the host systems designed airflow.

Table 28- Temperature Range Class of operation

Class	Case Temperature Range
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

SFP-DD/SFP-DD112/SFP112 are designed to allow for up to 48 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

Appendix A Normative Module and Connector Performance Requirements

A.1 Performance Tables

EIA-364-1000 [7] shall be used to define the test sequences and procedures for evaluating the connector system described in this document. Where multiple test options are available, the manufacturer shall select the appropriate option where not previously specified. The selected procedure should be noted when reporting data. If there are conflicting requirements or test procedures between EIA-364 procedures and those contained within this document, this document shall be considered the prevailing authority. Unless otherwise specified, procedures for sample size, data, and collection to be followed as specified in EIA-364-1000. See EIA-364-1000 Annex B for objectives of tests and test groups.

This document represents the minimum requirements for the defined product. Additional test conditions and evaluations may be conducted within the defined EIA-364-1000 sequences. More extreme test conditions and failure criteria may be imposed and still meet the requirements of this document.

Table 29 summarizes the performance criteria that are to be satisfied by the connector described in this document. Most performance criteria are validated by EIA-364-1000 testing, but this test suite leaves some test details to be determined. To ensure that testing is repeatable, these details are identified in Table 30. Finally, testing procedures used to validate any performance criteria not included in EIA-364-1000 are provided in Table 31.

Table 29- Form Factor Performance Requirements

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Plating Type	Plating type on connector contacts	Precious (refer to 7.6 for plating details)
Surface Treatment	Surface treatment on connector contacts; if surface treatment is applied, Test Group 6 is required	Manufacturer to specify
Wipe length	Designed distance a contact traverses over a mating contact surface during mating and resting at a final position. If less than 0.127 mm, test group 6 is required	Manufacturer to specify
Rated Durability Cycles	The expected number of durability cycles a component is expected to encounter over the course of its life	Connector/ cage: 100 cycles Module: 50 cycles
Mating Force[1]	Amount of force needed to mate a module with a connector when latches are deactivated	SFP112 module: 40 N MAX SFP-DD/SFP-DD112 module: 40 N MAX
Unmating Force[1]	Amount of forced needed to separate a module from a connector when latches are deactivated	SFP112 module: 12.5 N MAX SFP-DD/SFP-DD112 module: 30 N MAX
Latch Retention[1]	Amount of force the latching mechanism can withstand without unmating	SFP112 module: 90 N MIN SFP-DD/ SFP-DD112 module: 90 N MIN
Cage Latch Strength[1]	The amount of force that the cage latches can hold without being damaged.	100 N MIN
Cage Retention to Host Board[1]	Amount of force a cage can withstand without separating from the host board	SFP112 module: 100 N MIN SFP-DD/ SFP-DD112 module: 100 N MIN
Environmental Requirements		
Field Life	The expected service life for a component	10 years
Field Temperature	The expected service temperature for a component	65°C
Electrical Requirements		
Current	Maximum current to which a contact is exposed in use	0.5 A per signal contact MAX 1.5 A per power contact MAX
Operating Rating Voltage	Maximum voltage to which a contact is exposed in use	30 V DC per contact MAX

Note:
1. These performance criteria are not validated by EIA-364-1000 testing, see Table 31 for test procedures and pass/fail criteria.

Table 30 describes the details necessary to perform the tests described in the EIA-364-1000 test sequences. Testing shall be done in accordance with EIA-364-1000 and the test procedures it identifies in such a way that the parameters/ requirements defined in Table 29 are met. Any information in this table supersedes EIA-364-1000.

Table 30- EIA-364-1000 Test Details

Performance Parameters	Description/ Details	Requirements
Mechanical/ Physical Tests		
Durability (preconditioning)	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No evidence of physical damage
Durability[1]	EIA-364-09 To be tested with connector, cage, and module. Latches may be locked out to aid in automated cycling.	No visual damage to mating interface or latching mechanism
Environmental Tests		
Cyclic Temperature and Humidity	EIA-364-31 Method IV omitting step 7a Test Duration B	No intermediate test criteria
Vibration	EIA-364-28 Test Condition V Test Condition Letter D Test set-up: Connectors may be restrained by a plate that replicates the system panel opening as defined in this specification. External cables may be constrained to a non-vibrating fixture a minimum of 8 inches from the module. For cabled connector solutions: Wires may be attached to PCB or fixed to a non-vibrating fixture.	No evidence of physical damage -AND- No discontinuities longer than 1 µs allowed
Mixed Flowing Gas	EIA-364-65 Class II See Table 4.1 in EIA-364-1000 for exposure times Test option Per EIA-364-1000 option 3	No intermediate test criteria
Electrical Tests		
Low Level Contact Resistance[2]	EIA-364-23 20 mV DC Max, 100 mA Max To include wire termination or connector-to-board termination	20 mΩ Max change from baseline
Dielectric Withstanding Voltage	EIA-364-20 Method B 300 VDC minimum for 1 minute Applied voltage may be product / application specific	No defect or breakdown between adjacent contacts -AND- 1 mA Max Leakage Current

Notes:
1. If the durability requirement on the connector is greater than that of the module, modules may be replaced after their specified durability rating.
2. The first low level contact resistance reading in each test sequence is used to determine a baseline measurement. Subsequent measurements in each sequence are measured against this baseline.

Table 31 describes the testing procedures necessary to validate performance criteria not validated by EIA-364-1000 testing. The tests are to be performed in such a way that the parameters/ requirements defined in Table 29 are met.

Table 31- Additional Test Procedures

Tests	Test Descriptions and Details	Pass/ Fail Criteria's
Mechanical/ Physical Tests		
Mating Force[1]	EIA-364-13 Mating/ unmating rate 12.7 mm/min To be tested with cage, connector, and module. Latching mechanism deactivated (locked out).	Refer to Table 29 -AND- No physical damage to any components
Unmating Force[1]		
Latch Retention[1]	EIA-364-13 Mating/ unmating rate 12.7 mm/min To be tested with cage, connector, and module. Latching mechanism engaged (not locked out).	
Latch Strength	An axial load applied using a static load or ramped loading to the specified load. To be tested with cage, connector, and module or module representative tool without heat sinks Latching mechanism engaged (not locked out).	
Cage Retention to Host Board	Tested with module, module analog, or fixtures mated to cage. Pull cage in a direction perpendicular to the board at a rate of 25.4 mm/min to the specified force.	No physical damage to any components -AND- Cage shall not separate from board
Electrical Tests		
Current	EIA-364-70 Method 3, 30-degree temperature rise Contacts energized: All signal and power contacts energized simultaneously	Refer to Table 29 for current magnitude

Note:
1. Values listed in Table 29 apply with or without the presence of a riding heat sink.

1
2

End of Document