Finisar FTL4C3QE1C-20-FL Quick Spec:

Part Number:	FTL4C3QE1C-20-FL FTL4C3QE1C-20-EXT-FL FTL4C3QE1C-20-IND-FL
Form Factor:	QSFP
TX Wavelength:	1270nm-1330nm
Reach:	20km
Cable Type:	SMF
Rate Category:	40GBase
Interface Type:	CWDM-LR4
DDM:	Yes
Connector Type:	Dual-LC
Optical Power Budget:	9 dB
TX Power Min/Max:	-3 to +2.3 dBm
RX Power Min/Max:	-12 to +2.3 dBm

Product Features Finisar FTL4C3QE1C-20-FL

- Compliant to the IEEE 802.3ba(40GBASE-LR4)
- Compliant to the QSFP+ MSA SFF-8436 specification
- Up to 20km over SMF
- DFBs and PIN monitor photodiodes array for transmitter section
- PIN detectors and TIAs array for receiver section
- Four 10Gbps CWDM channels in the 1310nm band
- I^2C interface with integrated Digital Diagnostic Monitoring (DDM)
- Utilizes two standard LC optical connector
- Operating case temperature:
  - Standard: 0°C to +70 °C
  - Extended -5°C to +85 °C
  - Industrial -40°C to +85 °C

Applications Finisar FTL4C3QE1C-20-FL

- Extended 40GBASE-LR4 Ethernet links
- Infiniband QDR and DDR interconnects client-side
- 40G Telecom connections

Overview Finisar FTL4C3QE1C-20-FL

The FTL4C3QE1C-20-FL is a transceiver module designed for 20km optical communication applications. The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10Gbps electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be used. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Diagram

This product converts the 4-channel 10 Gbps electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40 Gbps data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gbps channels with different wavelengths. Each wavelength is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

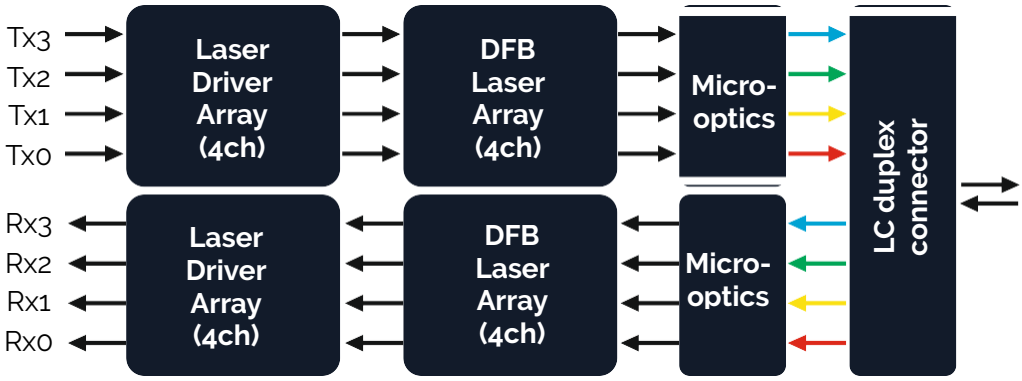


Figure 1. Functional diagram

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Tst*	-40	+85	°C
Relative Humidity (non-condensation)	RH	5	85	%
Operating Case Temp (Standard)	*Topc*	0	70	°C
Operating Case Temp (Industrial)	*Topc*	-40	85	°C

Recommended Operating Conditions

Parameter	Symbo	l	Min	Typ	Max	Unit
Power Supply Voltage	*Vcc*		3.15	3.3	3.45	V
Power Supply Current	*Icc*				1000	mA
Power Dissipation	*PD*				3.5	W
Aggregate Bit Rate	*BRAVE*			41.25		Gbps
Lane Bit Rate	*BRLANE*			10.3125		Gbps

Electrical Characteristics – Transmitter

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Single ended input voltage tolerance			-0.3		4	V	Referred to TP1 signal common
AC common mode input voltage tolerance			15			mV	RMS
Input Impedance (Differential)		*Zin*	85	100	115	ohms	Rin > 100 kohms @ DC
TX Disable	Disable	*VIH*	2		Vcc+0.3	V	
	Enable	*VIL*	0		0.8		
TX FAULT	Fault	*VOH*	2.4		Vcc+0.3	V	
	Normal	*VOL*	0		0.8		

Electrical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single ended output voltage		-0.3		4	V	Referred to signal common
AC common mode voltage				7.5	mV	RMS
Termination mismatch at 1MHz				5	%	
Output Impedance (Differential)	*Zout*	85	100	115	ohms	
Output Rise/Fall Time	*tr/tf*	30			ps	10%~90%
LOS	*VoH*	2.4		Vcc+0.3	V	
RX_LOS						
Normal	*VoL*	0		0.8	V	

Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SMF	L		20		km
Aggregate Bit Rate	*BRAVE*		41.25		Gbps
Per Lane Bit Rate	*BRLANE*		10.3125		Gbps

Optical Characteristics – Transmitter

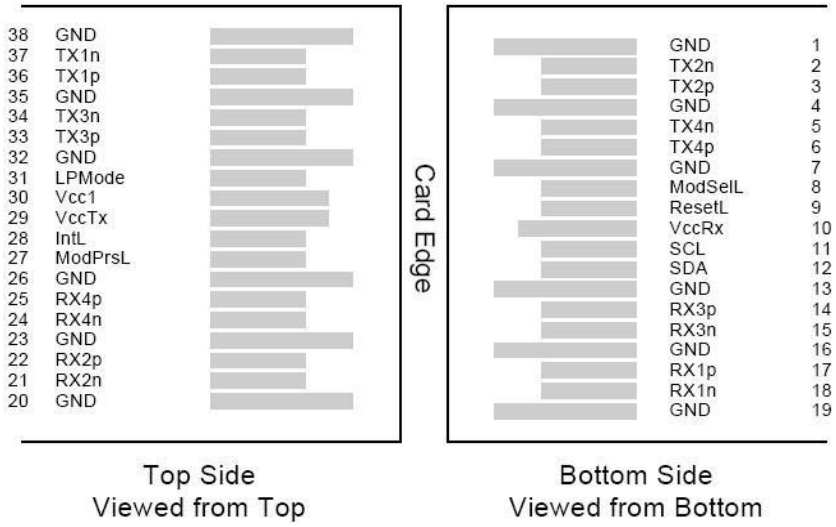
Parameter	Symbol	Min	Typ	Max	Unit
Channels wavelength	λC	1264.5	1271	1277.5	nm
		1284.6	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
-20dB spectral width	Δλ			1	Nm
Average Launch Power, Each Lane	*Pout/lane*	-3		2.3	dBm
Per Lane Bit Rate	*Er*	3.5			
Output Optical Eye		IEEE 802.3ba-2010 Compliant			

Optical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Channels wavelength	λC	1264.5	1271	1277.5	nm
		1284.6	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Damage Threshold		3.3			dBm
Receiver sensitivity in OMA, each lane	*Pmins*			-12	dBm
Maximum Receive Power, each lane	*Pmax*	2.3			dBm
Receiver reflectance	*Rr*			-26	Db
LOS De-Assert	*LOSD*			-11.5	dBm
LOS Assert	*LOSA*	-20			dBm

PIN Assignment and Function Definitions

PIN Assignment



PIN Definition

PIN	Signal Name	Description
1	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input
4	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input
7	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select
9	ResetL	LVTLL-I Module Reset
10	$V_{CC}Rx$	+3.3V Power Supply Receiver (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data
13	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output
15	Rx3n	CML-O Receiver 3 Inverted Data Output
16	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output
18	Rx1n	CML-O Receiver 1 Inverted Data Output
19	GND	Ground (1)
20	GND	Ground (1)
21	Rx2n	CML-O Receiver 2 Inverted Data Output
22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
23	GND	Ground (1)
24	Rx4n	CML-O Receiver 4 Inverted Data Output
25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
26	GND	Ground (1)
27	ModPrsL	Module Present
28	IntL	Interrupt
29	$V_{CC}Tx$	+3.3V Power Supply Transmitter (2)
30	VCC1	+3.3V Power Supply
31	LPMode	LVTLL-I Low Power Mode
32	GND	Ground (1)
33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
34	Tx3n	CML-I Transmitter 3 Inverted Data Input
35	GND	Ground (1)
36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
37	Tx1n	CML-I Transmitter 1 Inverted Data Input
38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. $V_{CC}Rx$, Vcc1 and $V_{CC}Tx$ are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

Licensing

The following U.S. patents are licensed by Finisar to FluxLight, Inc.:
U.S. Patent Nos: 7,184,668, 7,079,775, 6,957,021, 7,058,310, 6,952,531, 7,162,160, 7,050,720