# Quick Spec:

| | |
|---|---|
| Part Number: | 407-BCIB-FL<br>407-BCIB-EXT-FL<br>407-BCIB-IND-FL |
| Form Factor: | QSFP-DD |
| TX Wavelength: | 1310nm |
| Reach: | 2km |
| Cable Type: | SMF |
| Rate Category: | 400GBase |
| Interface Type: | FR4 |
| DDM: | Yes |
| Connector Type: | Dual-LC |

## Dell Compatible 407-BCIB-FL Features

- QSFP-DD MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- 100G Lambda MSA 400G-FR4 Specification compliant
- Up to 2km transmission on single mode fiber (SMF) with FEC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel.
- Maximum power consumption 12W
- Duplex LC connector
- RoHS compliant
- Operating Case Temperature
  - Standard: 0°C to +70 °C
  - Extended -5°C to +85 °C
  - Industrial -40°C to +85 °C

## Dell Compatible 407-BCIB-FL Applications

- Data Center Interconnect
- 400G Ethernet
- Infiniband interconnects
- Enterprise networking

## Dell Compatible 407-BCIB-FL General Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## Dell Compatible 407-BCIB-FL Functional Description

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver and EML lasers together with an optical multiplexer. On the receiver path, an optical de- multiplexer is coupled to a 4-channel photodiode array. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and also an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to IEEE 802.3bs with duplex LC connector.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2- wire serial communication commands. The ModSelL allows the use of this product on a single 2- wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low

## Transceiver Block Diagram

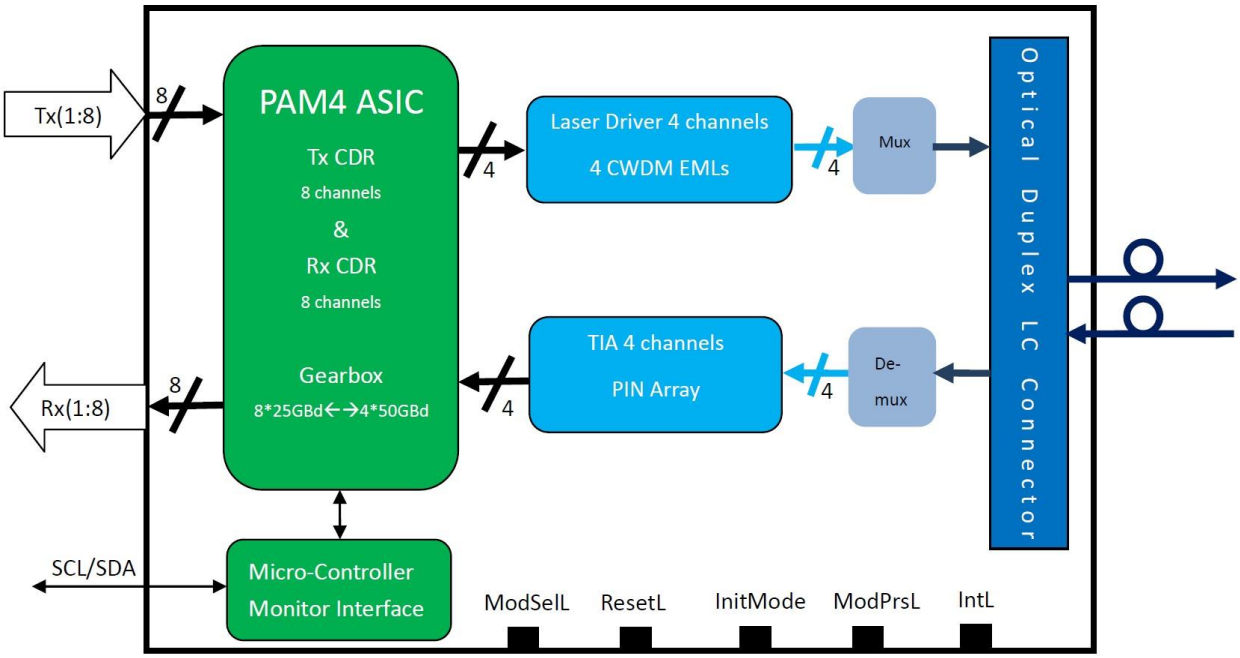



**Figure 1. Transceiver Block Diagram**

## Pin Assignment and Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

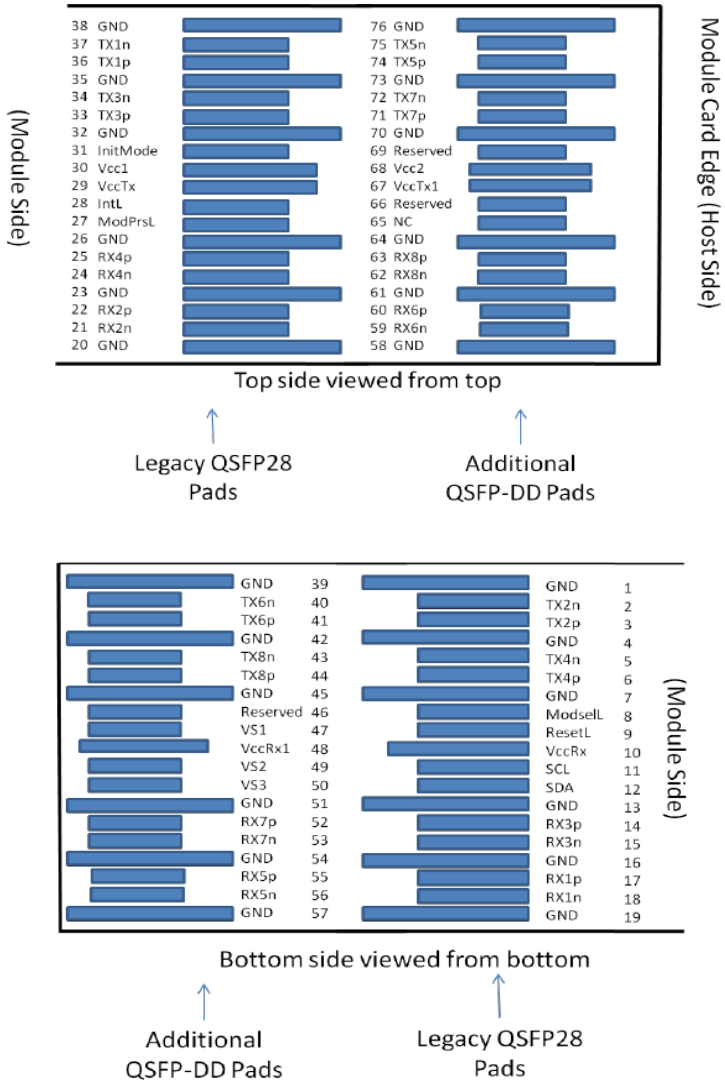



**Figure 2. MSA Compliant Connector**

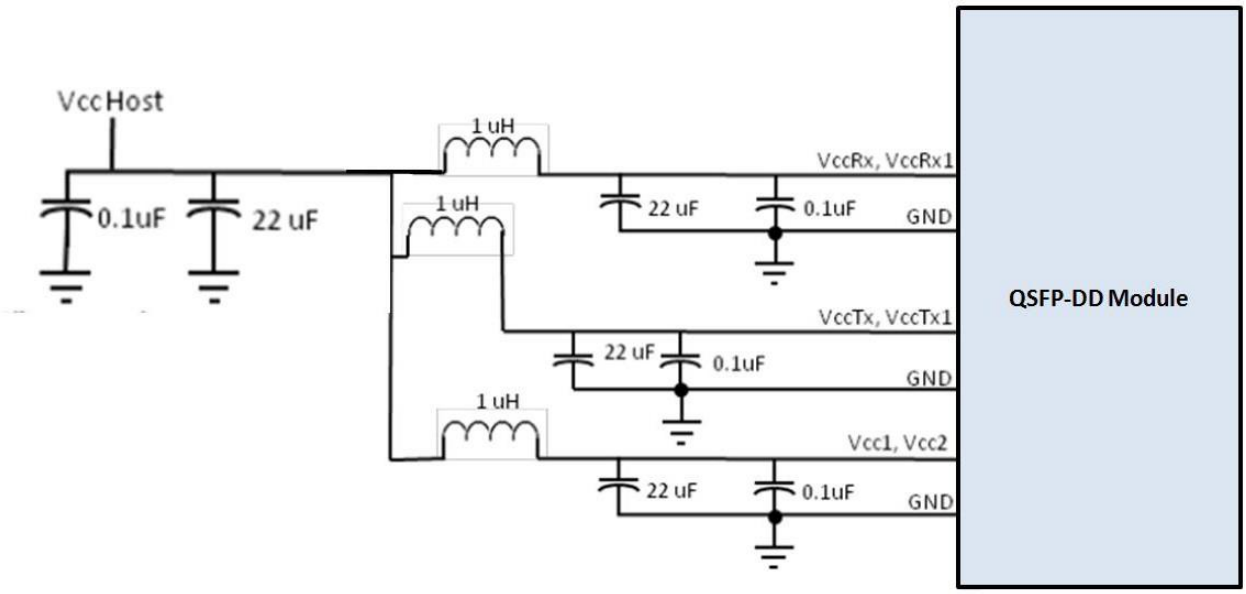
## Pin Definition

| Pin | Logic | Symbol | Description | Plug Sequence |
|---|---|---|---|---|
| 1 | | GND | Ground | 1B |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B |
| 4 | | GND | Ground | 1B |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B |
| 7 | | GND | Ground | 1B |
| 8 | LVTTL-I | ModSelL | Module Select | 3B |
| 9 | LVTTL-I | ResetL | Module Reset | 3B |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3B |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3B |
| 13 | | GND | Ground | 1B |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B |
| 16 | GND | Ground | 1B | |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B |
| 19 | | GND | Ground | 1B |
| 20 | | GND | Ground | 1B |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B |
| 23 | | GND | Ground | 1B |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B |
| 26 | | GND | Ground | 1B |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B |
| 28 | LVTTL-O | IntL | Interrupt | 3B |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B |
| 30 | | Vcc1 | +3.3V Power supply | 2B |
| 31 | LVTTL-I | InitMode | Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE | 3B |
| 32 | | GND | Ground | 1B |

| | | | | |
|---|---|---|---|---|
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B |
| 35 | | GND | Ground | 1B |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B |
| 38 | | GND | Ground | 1B |
| 39 | | GND | Ground | 1A |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A |
| 42 | | GND | Ground | 1A |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A |
| 45 | | GND | Ground | 1A |
| 46 | | Reserved | For future use | 3A |
| 47 | | VS1 | Module Vendor Specific 1 | 3A |
| 48 | | VccRx1 | 3.3V Power Supply | 2A |
| 49 | | VS2 | Module Vendor Specific 2 | 3A |
| 50 | | VS3 | Module Vendor Specific 3 | 3A |
| 51 | | GND | Ground | 1A |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A |
| 54 | | GND | Ground | 1A |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A |
| 57 | | GND | Ground | 1A |
| 58 | | GND | Ground | 1A |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A |
| 61 | | GND | Ground | 1A |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A |
| 64 | | GND | Ground | 1A |
| 65 | | NC | No Connect | 3A |
| 66 | | Reserved | For future use | 3A |
| 67 | | VccTx1 | 3.3V Power Supply | 2A |
| 68 | | Vcc2 | 3.3V Power Supply | 2A |
| 69 | | Reserved | For Future Use | 3A |
| 70 | | GND | Ground | 1A |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A |

| | | | | |
|---|---|---|---|---|
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A |
| 73 | | GND | Ground | 1A |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A |
| 76 | | GND | Ground | 1A |

## Recommended Power Supply Filter



## Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | 85 | degC | |
| Operating Case Temperature – Commercial | $T_{OP}$ | 0 | 70 | degC | |
| Operating Case Temperature – Industrial | $T_{OP}$ | -40 | 85 | degC | |
| Power Supply Voltage | $V_{CC}$ | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |

## Recommended Operating Conditions and Power Supply Requirements

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | TOP | 0 | | 70 | degC | |
| Power Supply Voltage | VCC | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 26.5625 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | $2.4x10^{-4}$ | | |
| Post-FEC Bit Error Ratio | | | | $1x10^{-12}$ | | 1 |
| Link Distance | D | 0.5 | | 10 | km | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

## Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Test Point | Min | Typical | Max | Units | Parameter |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 12 | W | Power Consumption |
| Supply Current | Icc | | | 3.64 | A | Supply Current |
| Transmitter (each Lane) | | | | | | |
| Signaling Rate, each Lane | TP1 | | 26.5625 ± 100 ppm | | GBd | |
| Differential pk-pk Input Voltage | TP1a | 900 | | | mVpp | 1 |
| Differential Termination Mismatch | TP1 | | | 10 | % | |
| Differential Input Return Loss | TP1 | IEEE 802.3-2015 Equation (83E-5) | | | dB | |
| Differential to Common Mode Input Return Loss | TP1 | IEEE 802.3-2015 Equation (83E-6) | | | dB | |
| Module Stressed Input Test | TP1a | See IEEE 802.3bs 120E.3.4.1 | | | | 2 |
| Single-ended Voltage Tolerance Range (Min) | TP1a | -0.4 to 3.3 | | | V | |
| DC Common Mode Input Voltage | TP1 | -350 | | 2850 | mV | 3 |
| **Receiver (each Lane)** | | | | | | |
| Signaling Rate, each lane | TP4 | | 26.5625 ± 100 ppm | | GBd | |
| Differential Peak-to-Peak Output Voltage | TP4 | | | 900 | mVpp | |
| AC Common Mode Output Voltage, RMS | TP4 | | | 17.5 | mV | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Differential Output Return Loss | TP4 | IEEE 802.3-2015 Equation (83E-2) | | | | |
| Common to Differential Mode Conversion Return Loss | TP4 | IEEE 802.3-2015 Equation (83E-3) | | | | |
| Transition Time, 20% to 80% | TP4 | | 9.5 | | ps | |
| Near-end Eye Symmetry Mask Width (ESMW) | TP4 | | | 0.265 | UI | |
| Near-end Eye Height, Differential | TP4 | | 70 | | mV | |
| Far-end Eye Symmetry Mask Width (ESMW) | TP4 | | | 0.2 | UI | |
| Far-end Eye Height, Differential | | | 30 | | mV | |
| Far-end Pre-cursor ISI Ratio | | | -4.5 | | 2.5 % | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Common Mode Output Voltage (Vcm) | | | -350 | | 2850 | mV | 3 |

Notes:

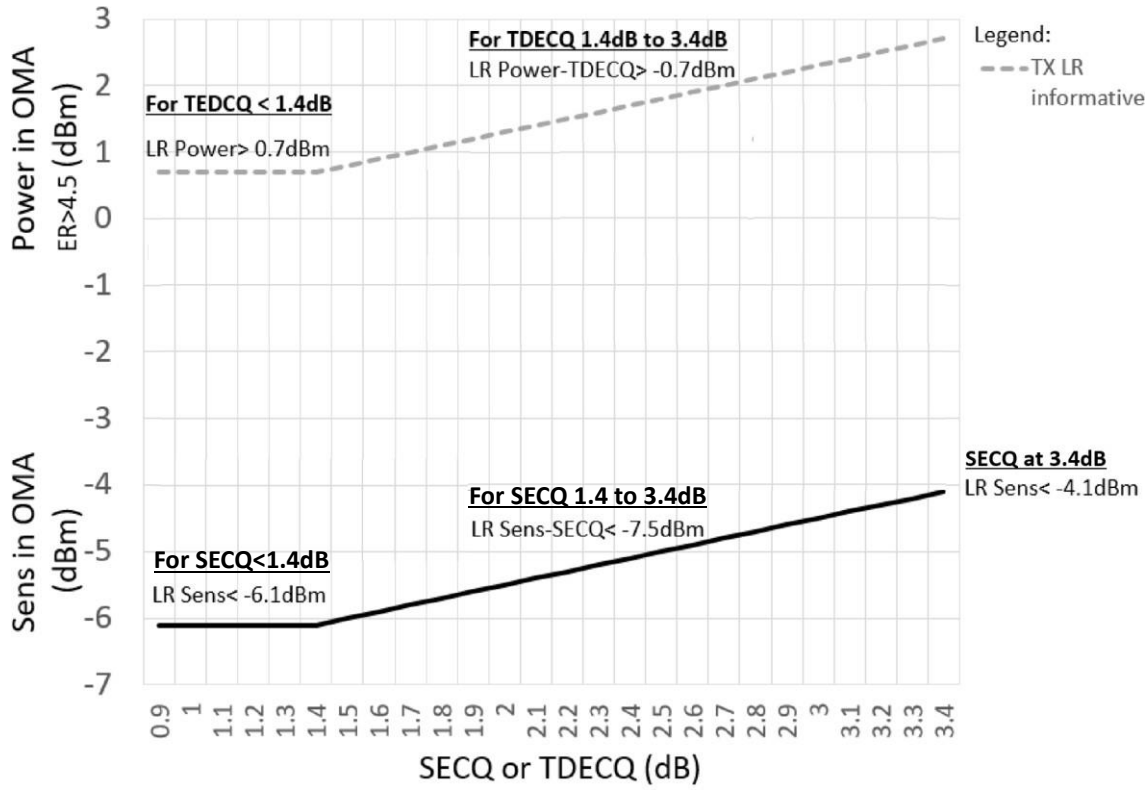
1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

## Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Wavelength Assignment | L0 | 1264.5 | 1271 | 1277.5 | nm | |
| | L1 | 1284.5 | 1291 | 1297.5 | nm | |
| | L2 | 1304.5 | 1311 | 1317.5 | nm | |
| | L3 | 1324.5 | 1331 | 1337.5 | nm | |
| **Transmitter** | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | Modulated |
| Total Average Launch Power | PT | | | 9.3 | dBm | |
| Average Launch Power, each Lane | PAVG | -3.3 | | 3.5 | dBm | 1 |
| Outer Optical Modulation Amplitude ($OMA_{outer}$), each Lane | POMA | -0.3 | | 3.7 | dBm | 2 |
| Launch Power in $OMA_{outer}$ minus TDECQ, each Lane | | -1.7 | | | dB | For ER ≥4.5dB |
| Launch Power in $OMA_{outer}$ minus TDECQ, each Lane | | -1.6 | | | dB | For ER <4.5dB |
| Transmitter and Dispersion Eye Clouser for PAM4, each Lane | TDECQ | | | 3.4 | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| Difference in Launch Power between any Two Lanes ($OMA_{outer}$) | | | | 4 | dB | |
| $RIN_{17.1}OMA$ | RIN | | | -136 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 17.1 | dB | |
| Transmitter Reflectance | TR | | | -26 | dB | |
| Average Launch Power of OFF Transmitter, each Lane | $P_{off}$ | | | -20 | dBm | |
| **Receiver** | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Damage Threshold, each Lane | $TH_d$ | 5.5 | | | dBm | 3 |
| Average Receive Power, each Lane | | -7.7 | | 4.5 | dBm | 4 |
| Receive Power ($OMA_{outer}$), each Lane | | | | 4.7 | dBm | |
| Difference in Receiver Power between any Two Lanes ($OMA_{outer}$) | | | | 4.1 | dB | |
| Receiver Sensitivity ($OMA_{outer}$), each Lane | SEN | | | -6.6 | dBm | For BER of 2.4E-4 |
| Stressed Receiver Sensitivity ($OMA_{outer}$), each Lane | SRS | See Figure 4 | | | dBm | 5 |
| Receiver Reflectance | RR | | | -26 | dB | |
| LOS Assert | LOSA | -30 | | | dBm | |
| LOS De-assert | LOSD | | | -12 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Stressed Conditions for Stress Receiver Sensitivity (Note 6) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | 0.9 | | 3.4 | dB | |
| $OMA_{outer}$ of each Aggressor Lane | | | 1.5 | | dBm | |

1. Notes:
2. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the $OMA_{outer}$ (min) must exceed the minimum value specified here.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Measured with conformance test signal for BER = $2.4 \times 10^{-4}$. A compliant receiver shall have stressed receiver sensitivity ($OMA_{outer}$), each lane values below the mask of Figure 4, for SECQ values between 0.9 and 3.4 dB.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver



## Digital Diagnostic Functions

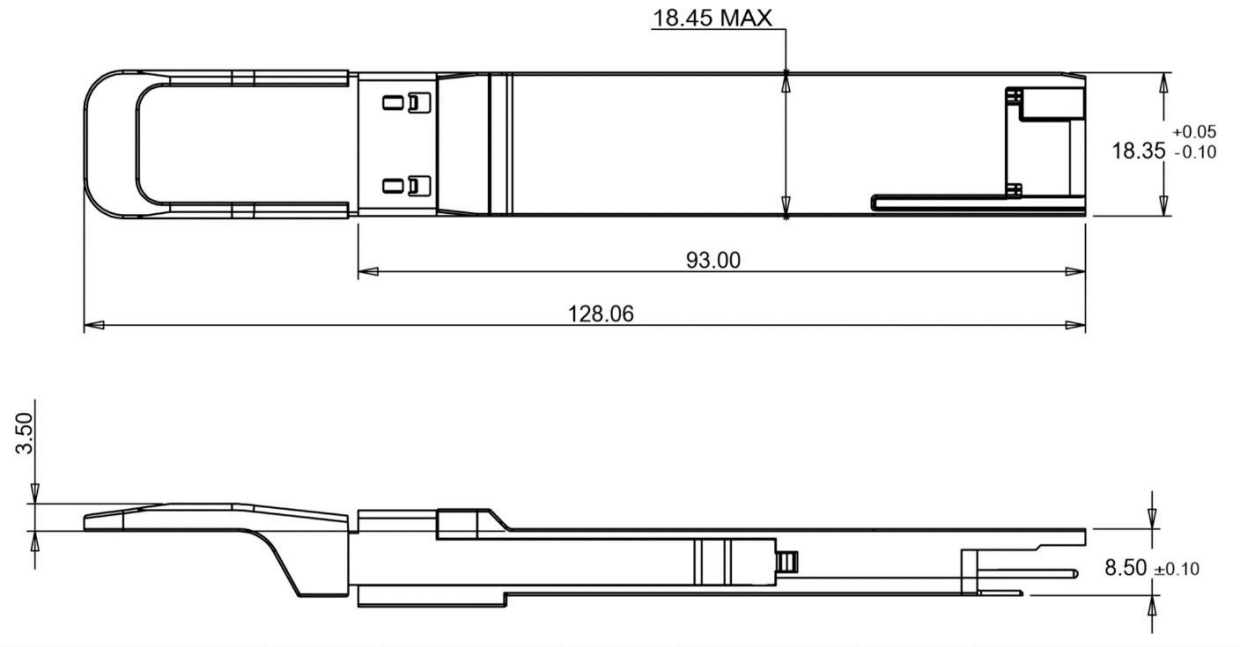
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI _VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor bsolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor bsolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

## Mechanical Dimensions




## ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22- A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).
Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Licensing

The following U.S. patents are licensed by Finisar to FluxLight, Inc.:
U.S. Patent Nos: 7,184,668, 7,079,775, 6,957,021, 7,058,310, 6,952,531, 7,162,160, 7,050,720