Part Number: 40G-QSFP-ER4

OVERVIEW

The 40G-QSFP-ER4 is a transceiver module designed for 30km optical communication applications. The design is compliant to 40GBASE-ER4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10 Gbps electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40 Gbps optical transmission. Reversely, on the receiver side, the module optically demultiplexes a 40Gbps input into 4 CWDM channels signals, and converts them to 4 channel output electrical data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be used. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

PRODUCT FEATURES

- Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-ER4 Standard
- QSFP+ MSA compliant
- Compliant with QDR/DDR Infiniband data rates
- Up to 11.2Gb/s data rate per wavelength
- 4 CWDM lanes MUX/DEMUX design
- Up to 30km transmission on single mode fiber (SMF)
- Operating case temperature: 0 to 70°C
- Maximum power consumption 3.5W
- LC duplex connector
- RoHS compliant

APPLICATIONS

- 40GBASE-ER4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Client-side 40G Telecom connections

FUNCTIONAL DIAGRAM

This product converts the 4-channel 10 Gbps electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40 Gbps data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gbps channels with different wavelengths. Each wavelength is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier. Figure 1 shows the functional block diagram of this product. A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.
Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

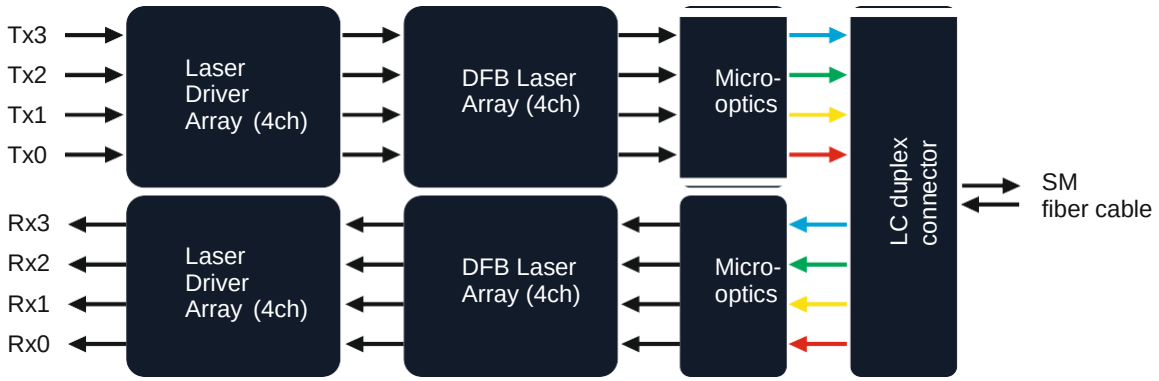


Figure 1. Functional diagram

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.
Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.
Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.
Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

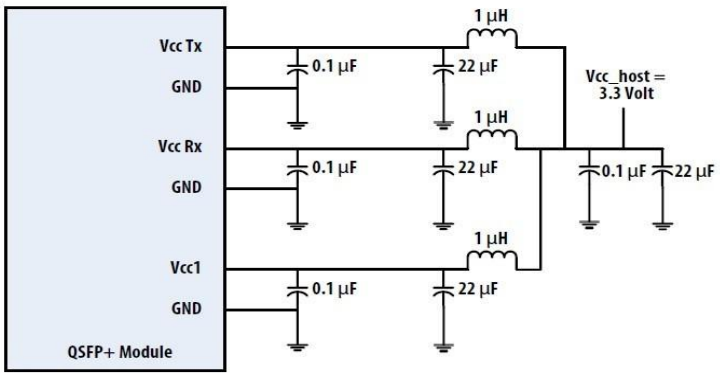
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Ts*	-40	+85	degC
Operating Case Temperature	*Top*	0	70	degC
Power Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensation)	*RH*	0	85	%
Damage Threshold, each Lane	*THd*	3.8		dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	*TOP*	0		70	degC
Power Supply Voltage	*Vcc*	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance with G652	D			30	km

RECOMMENDED POWER SUPPLY FILTER



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Power Consumption				3.5	W
Supply Current	*Icc*			1.1	A
Transceiver Power-on Initialization Time (Note 1)				2000	ms

ELECTRICAL CHARACTERISTICS – TRANSMITTER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance (RMS)		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	$V_{in,pp}$	190		700	mV_{pp}	
Differential Input Impedance	Z_{in}	90	100	110	Ω	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.1.1			dB	10MHz - 11.1GHz
J2 Jitter Tolerance	J_{t2}	0.17			UI	
J9 Jitter Tolerance	J_{t9}	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance		0.07			UI	
Eye Mask Coordinates {X1, X2,		0.11, 0.31			UI	Hit Ratio = $5x10^{-5}$
Y1, Y2}		95, 350			mV	

ELECTRICAL CHARACTERISTICS – RECEIVER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single-ended Output Voltage Threshold		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage Tolerance (RMS)				7.5	mV	RMS
Differential Output Voltage Swing Threshold	$V_{out,pp}$	300		850	mV_{pp}	
Differential Output Impedance	A_{out}	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss		See IEEE 802.3ba 86A.4.2.1			dB	10MHz - 11.1GHz
Common mode Output Return Loss		See IEEE 802.3ba 86A.4.2.2			dB	10MHz - 11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Tolerance	J_{o2}			0.42	UI	
J9 Jitter Tolerance	J_{o9}			0.65	UI	
Eye Mask Coordinates {X1, X2,		0.29, 05			UI	Hit Ratio = $5x10^{-5}$
Y1, Y2}		150, 425			mV	

Notes:

1. Power-on initialization time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the moduleis fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

OPTIICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength Assignment	λ_0	1264.5	1271	1277.5	nm
	λ_1	1284.5	1291	1297.5	nm
	λ_2	1304.5	1311	1317.5	nm
	λ_3	1324.5	1331	1337.5	nm

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Side Mode Suppression Ratio	*SMSR*	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power (each Lane)	P_{AVG}	-3.7		4.5	dBm	
Optical Modulation Amplitude (OMA) (each Lane)	P_{OMA}	-0.7		5	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	$P_{tx,diff}$			4.7	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-1.5			dBm	
TDP, each Lane	*TDP*			2.6	dB	
Extinction Ratio	*ER*	5.5			dB	
Relative Intensity Noise	*RIN*			-128	dB/Hz	12dB reflection
Transmitter Reflectance	R_T			-12	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OFF (each Lane)	P_{off}			-30	dBm	

Note: Transmitter optical characteristics are measured with a single mode fiber.

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Damage Threshold, each Lane	$_{THd}$	3.8			dBm	2
Average Receive Power, each Lane		-20.2		-1.5	dBm	
Receiver Reflectance	R_R			-26	dB	
Receive Power (OMA) (each Lane)				-1	dBm	
Receiver Sensitivity in OMA (each Lane)	*SEN*			-18	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-15.8	dBm	3
Difference in Receive Power between any 2 Lanes (OMA)	$P_{RX,diff}$			7	dB	
LOS Assert	LOS_A	-35			dBm	
LOS Deassert	LOS_D			-20	dBm	
LOS Hysteresis	LOS_H	0.5			dB	
Receiver Electrical 3dB upper cut-off Frequency (each Lane)	F_c			12.3	GHz	
Vertical Eye Closure Penalty, each Lane			2.2		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:

1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Measured with conformance test signal at receiver input for BER = 1x10-12.
4. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
5.

DIGITAL DIAGNOSTIC FUNCTIONS

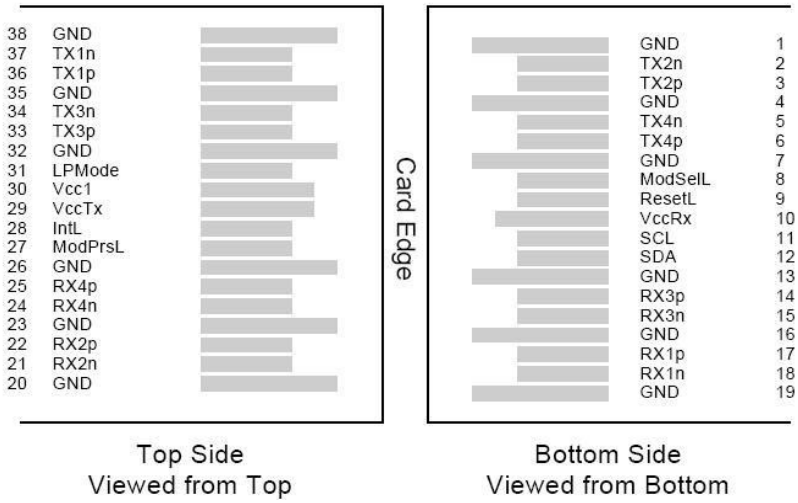
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_{TEMP}	-3		3	deg. C	Over operating temperature range
Supply voltage monitor absolute error	DMI_{VCC}	-0.1		0.1	V	Over Full operating range
Channel RX power monitor absolute error	DMI_{RX_CH}	-2		2	dB	1
Channel Bias current monitor	DMI_{Ibias_CH}	-10%		10%	mA	
Channel TX power monitor absolute error	DMI_{TX_CH}	-2		2	dB	1

Note 1: Due to measurement accuracy of different multi-mode fibers, there could be an additional ±1dB fluctuation, or ± 3dB total accuracy.

PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN Assignment

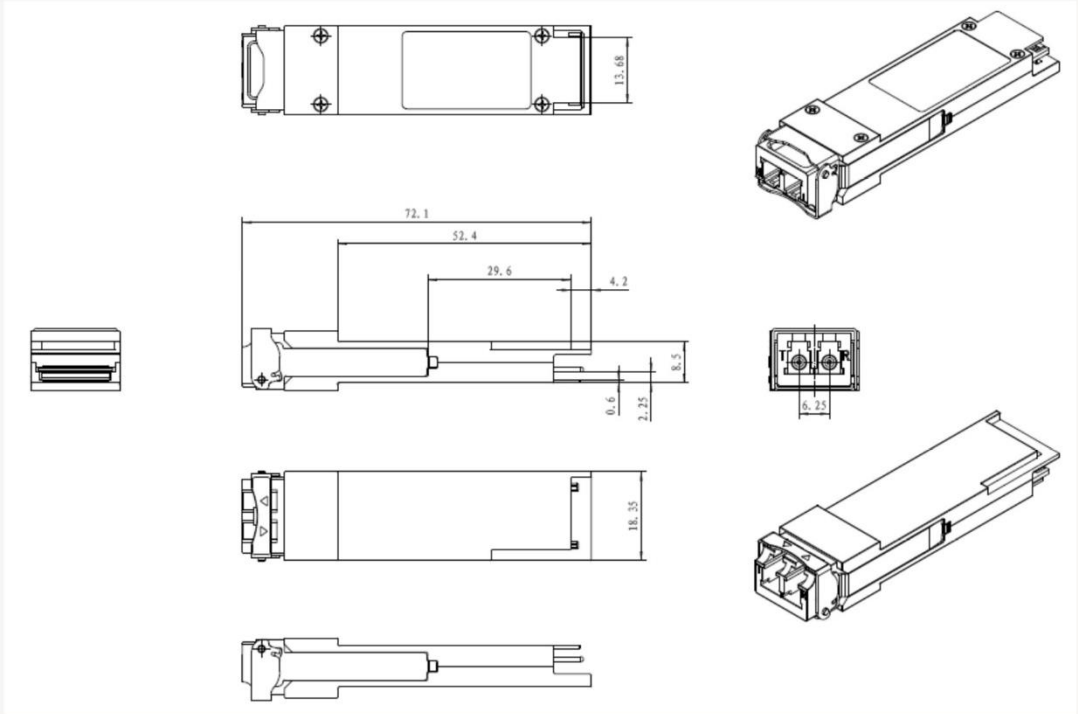


PIN Definition

PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	Ground (1)	20	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	21	Rx2n	CML-O Receiver 2 Inverted Data Output
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
4	GND	Ground (1)	23	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	24	Rx4n	CML-O Receiver 4 Inverted Data Output
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
7	GND	Ground (1)	26	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select	27	ModPrsL	Module Present
9	ResetL	LVTLL-I Module Reset	28	IntL	Interrupt
10	$V_{CC}R_x$	+3.3V Power Supply Receiver (2)	29	$V_{CC}Tx$	+3.3V Power Supply Transmitter (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock	30	$V_{CC}1$	+3.3V Power Supply
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data	31	LPMode	LVTLL-I Low Power Mode
13	GND	Ground (1)	32	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
15	Rx3n	CML-O Receiver 3 Inverted Data Output	34	Tx3n	CML-I Transmitter 3 Inverted Data Input
16	GND	Ground (1)	35	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input

18	Rx1n	CML-O Receiver 1 Inverted Data Output	37	Tx1n	CML-I Transmitter 1 Inverted Data Input
19	GND	Ground (1)	38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{cc}Rx, Vcc1 and V_{cc}Tx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

MECHANICAL DRAWING