Arista Compatible Compatible QSFP-40G-PLRL4 Quick Spec:

Part Number:	QSFP-40G-PLRL4 QSFP-40G-PLRL4-IND
Form Factor:	QSFP
TX Wavelength:	1310nm
Reach:	1.4km
Cable Type:	SMF
Rate Category:	40Gbase
Interface Type:	IR4-PSM
DDM:	Yes
Connector Type:	MPO
Optical Power Budget:	7.4dB
TX Power Min/Max:	-5.20 to +0.50 dBm
RX Power Min/Max:	-12.6 to 0.50 dBm

Arista Compatible Compatible QSFP-40G-PLRL4 Product Features

- 4 Parallel lanes design
- Up to 11.2Gbps data rate per channel
- Aggregate bandwidth of up to 40G
- QSFP+ MSA compliant
- Up to 1.5km transmission
- Maximum 3.5W operation power
- Single +3.3V power supply
- Operating case temperature:
  - Standard: 0~70 °C
  - Industrial -40 to +85 °C
- RoHS-6 compliant

Arista Compatible Compatible QSFP-40G-PLRL4 Applications

- 40G Ethernet
- Infiniband QDR, DDR and SDR
- Switch Router and HBA's
- High-performance Backplane
- Datacenter and Enterprise networking

Arista Compatible Compatible QSFP-40G-PLRL4 Overview

The QSFP-40G-PLRL4 is a parallel 40 Gbps Quad Small Form-factor Pluggable (QSFP+) optical module. It provides increased port density and total system cost savings. The QSFP+ full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10 Gbps operation for an aggregate data rate of 40 Gbps over 1.5km of single mode fiber. An optical fiber ribbon cable with an MPO/MTPTM connector can be plugged into the QSFP+ module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a z-pluggable 38-pin connector. The module operates via a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility. The «Part» design is compliant to QSFP+ Multi-source agreement (MSA) in terms of form factor, optical/electrical connection and digital diagnostic interface. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module can be managed through the I2C two-wire serial interface.

Arista Compatible Compatible QSFP-40G-PLRL4 Functional Diagram

This product converts the 4-channel 10 Gbps electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40 Gbps data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gbps channels with different wavelengths. Each wavelength is collected by a discrete avalanche photodiode (APD), and then outputted as electric data after amplified first by a TIA and then by a post amplifier. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

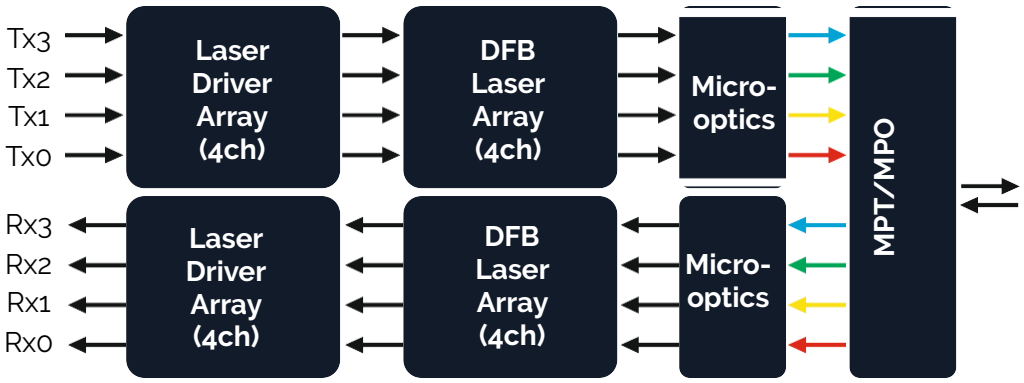


Figure 1. Functional diagram

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

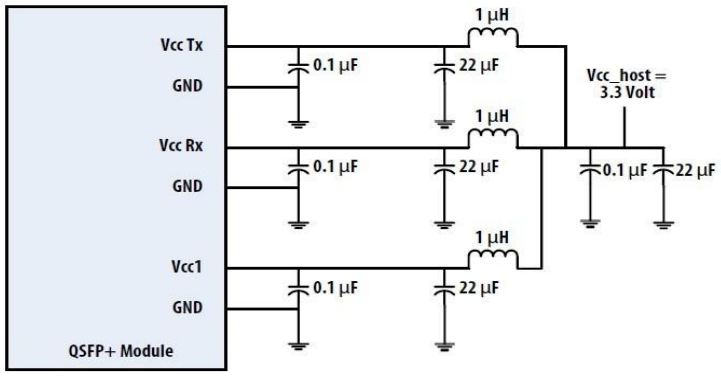
Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Ts*	-40	+85	°C
Relative Humidity	RH	0	85	%
Supply Voltage	*Vcc*	3.15	3.14	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature (Standard)	*Ts*	0		+70	°C
Storage Temperature (Industrial)	*Ts*	-40		+85	°C
Power Supply voltage	Vcc	3.15	3.3	3.45	V
Power Consumption		0		3.5	W
Data Rate	*DR*		10.3		Gbps
Data Speed tolerance	*LDR*	-100		100	Ppm
Link Distance with G652				15	Km

Recommended Power Supply Filter



Electrical Characteristics - Transmitter

Parameter	Symbol	Min	Typ	Max	Unit
Differential Input Impedance		90	100	110	Ohm
Differential Input Swing		190		700	mV
TP1/TP1a Interface		Compliant to IEEE 802.3ba XLPPI			

Electrical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Differential Output Impedance		90	100	110	Ohm
Termination Mismatch at 1MHz		300		850	mV
Output Differential Return Loss		Compliant to IEEE 802.3ba			dB

Optical Characteristics - Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Center Wavelength	$\lambda 0$	1260	1310	1360	nm	1
RMS Spectral Width	Λrms			3.5	nm	1
Average Launch Power	*Pavg*	-5.2	-2.5	+0.5	dBm	
Optical Modulation Amplitude (OMA) (each Lane)	P_{OMA}	-4.5	-2.5	+2.0	dBm	1
Launch Power in OMA minus Transmitter and dispersion Penalty (TDP), each lange	OMA-TDP	-9.7			dBm	1
Rise/Fall Time	Tr/Tf			50	Ps	
Extinction Ration	ER	3.5			dB	
Relative Intensity Noise	*RIN*			-128	dB/Hz	
Optical Return Lose Tolerance	*TOL*			12	dB	
Transmitter Reflectance	*RT*			-12	dB	
Transmitter Eye Mask Margin	*EMM*	5			%	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OF (each lane)	P_{off}			-30	dBm	

Note: Transmitter optical characteristics are measured with a single mode fiber.

Optical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Centre Wavelength	λ0	1260	1310	1360	nm	
Damage Threshold	Thd	+3			dBm	
Overload, (each Lane)	OVL	+0.5			dBm	
Receiver Sensitivity in OMA (each Lane)	SEN			-12.6	dBm	
Difference in Receive Power between any two Lanes (OMA)	Prx,diff			5.0	dB	
Signal Loss Assert Threshold	LOSA	-30			dBm	
Signal Loss Deassert Threshold	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5		6	dB	
Optical Return Loss	ORL			-12	dBm	
Receiver Electrical 3dB upper cut-off Frequency (each Lane)	Fc			12	GHz	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digitial Diagnostics Function

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMITEMP	-3		3	deg. C	Over operating temperature range
Supply voltage monitor absolute error	DMIVCC	-0.1		0.1	V	Over Full operating range
Channel RX power monitor absolute error	DMIRX_CH	-2		2	dB	1
Channel Bias current monitor	DMIIbias_CH	-10%		10%	mA	
Channel TX power monitor absolute error	DMITX_CH	-2		2	dB	1

Note 1: Due to measurement accuracy of different multi-mode fibers, there could be an additional ±1dB fluctuation, or ± 3dB total accuracy.

Mode-Conditioning Patch Cable

Figure 2. shows the orientation of the multi-mode facets of the optical connector.

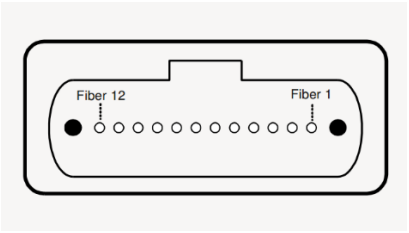
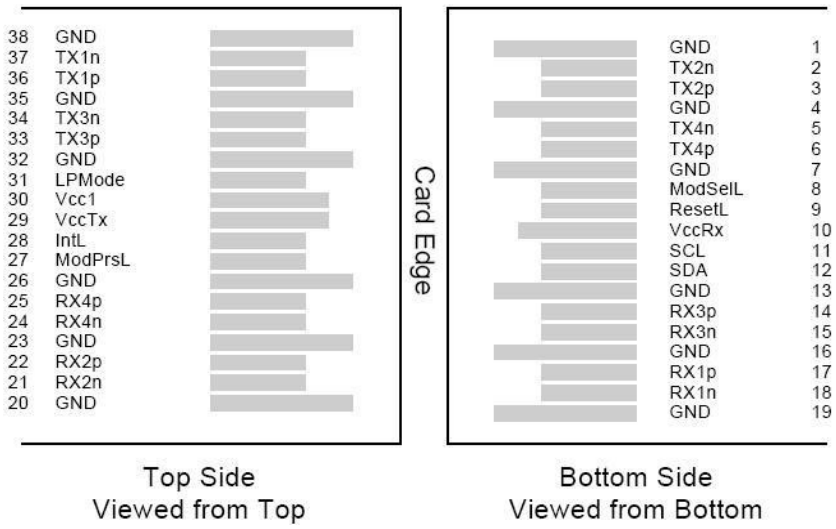


Figure 2. Optical connector

Fiber	Description	PIN	Description
1	Rx (0)	7	Not used
2	Rx (1)	8	Not used
3	Rx (2)	9	Tx (3)
4	Rx (3)	10	Tx (2)
5	Not used	11	Tx (1)
6	Not used	12	Tx (0)

PIN Assignment and Function Definitions

PIN Assignment



PIN Definition

PIN	Signal Name	Description
1	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input
4	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input
7	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select
9	ResetL	LVTLL-I Module Reset
10	VCCRx	+3.3V Power Supply Receiver (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data
13	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output
15	Rx3n	CML-O Receiver 3 Inverted Data Output
16	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output
18	Rx1n	CML-O Receiver 1 Inverted Data Output
19	GND	Ground (1)
20	GND	Ground (1)
21	Rx2n	CML-O Receiver 2 Inverted Data Output
22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
23	GND	Ground (1)
24	Rx4n	CML-O Receiver 4 Inverted Data Output
25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
26	GND	Ground (1)
27	ModPrsL	Module Present
28	IntL	Interrupt
29	VCCTx	+3.3V Power Supply Transmitter (2)
30	VCC1	+3.3V Power Supply
31	LPMode	LVTLL-I Low Power Mode
32	GND	Ground (1)
33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
34	Tx3n	CML-I Transmitter 3 Inverted Data Input
35	GND	Ground (1)
36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
37	Tx1n	CML-I Transmitter 1 Inverted Data Input
38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{CC}Rx, Vcc1 and V_{CC}Tx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.